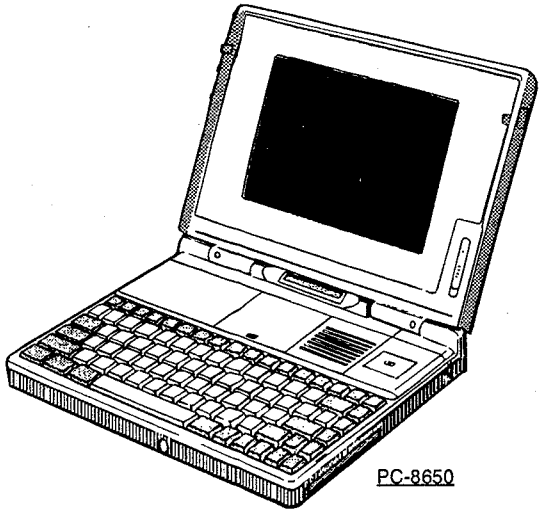
SHARP SERVICE MANUAL

CODE: 00ZPC8650SM-E


PC-8650

PERSONAL COMPUTER

PC-7850
PC-8150
MODEL PC-8650

CONTENTS

Parts marked with "⚠" is important for maintaining the safety of the set. Be sure to replace these parts with specified ones for maintaining the safety and performance of the set.

SHARP CORPORATION

【THE FOLLOWING CAUTION IS APPLICABLE IN THE UNITED STATES ONLY. 】
"B A T T E R Y D I S P O S A L"
"CONTAINS NICKEL-CADMIUM RECHARGEABLE BATTERY MUST BE RECYCLED OR DISPOSED OF PROPERLY. REMOVE THE BATTERY FROM THE PRODUCT AND CONTACT FEDERAL OR STATE ENVIRONMENTAL AGENCIES FOR INFORMATION ON RECYCLING AND DISPOSAL OPTIONS."

【THE FOLLOWING CAUTION IS APPLICABLE IN THE UNITED STATES ONLY. 】
"B A T T E R Y D I S P O S A L"
"CONTAINS NICKEL-METAL HYDRIDE RECHARGEABLE BATTERY MUST BE RECYCLED OR DISPOSED OF PROPERLY. REMOVE THE BATTERY FROM THE PRODUCT AND CONTACT FEDERAL OR STATE ENVIRONMENTAL AGENCIES FOR INFORMATION ON RECYCLING AND DISPOSAL OPTIONS."

Chapter 1. OUTLINE OF THE PC-8650/8150/7850

1. General

1-1. System Overview

In a compact notebook-sized package, the system packs an incredible volume of PC performance and versatility. In fact, the system is equipped with more features than are found on many desktop computers.
All the components of this machine are enclosed in a sturdy plastic case. The ports and connectors which the system uses to connect to peripheral items and other systems are located on the right, left and rear panels of the case.
Place the system on a desk or table where you can examine it easily. Look at the front, side and rear panels of the system before you actually open it up. This way it will be easier to spin the machine round and examine each side in detail.

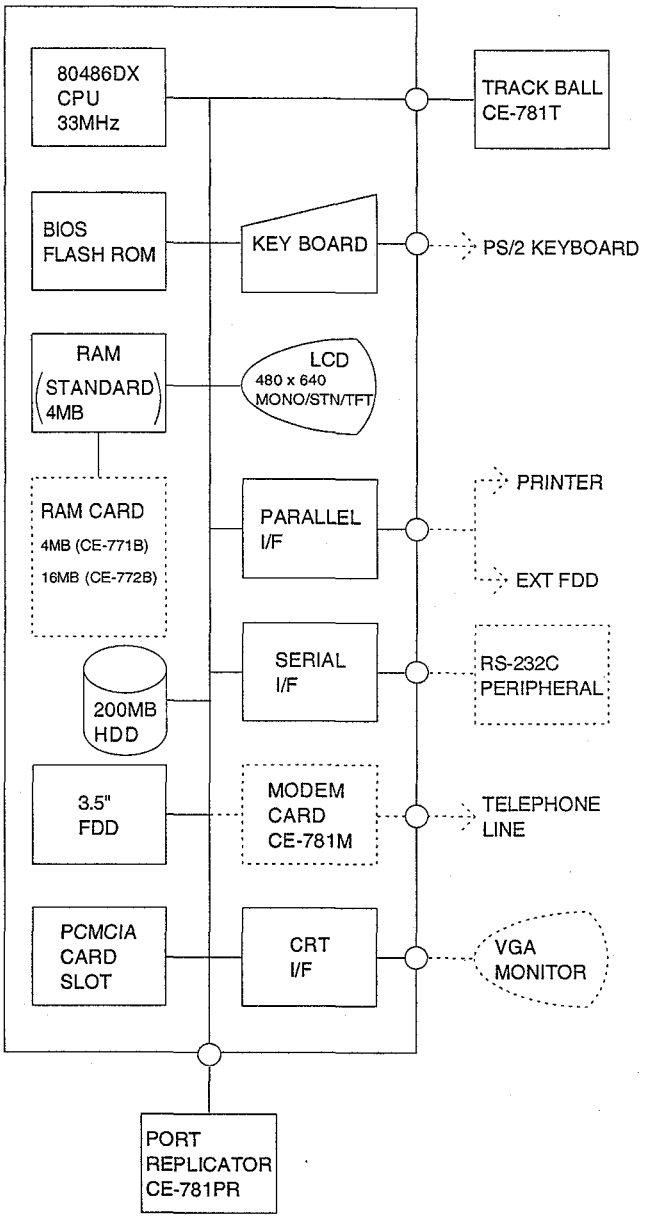
1-2. Feature Highlights

- Intel SL-Enhanced CPUi486DX-33MHz with SMM (System Management Mode)
- Standard 4MB RAM. Expandable up to 20MB
- Advanced power management features
- Power saving features
- Notebook-sized compact package

Device

- Monochrome LCD (640 x 480 dots) with backlight (PC-7850)
- Color STN-LCD (640 x 480 dots) with backlight (PC-8150)
- Color TFT-LCD (640 x 480 dots) with backlight (PC-8650)
- 3.5" 1.44MB/720KB Floppy Disk Drive
- 2.5" 200MB Hard Disk Drive
- PCMCIA Drive
- Optional External Trackball, a pointing device
- Optional I/O (Input/Output) Port Replicator
- Optional fax/modem card (Data Mode:14400bps, Fax Mode: 14400bps)
- Optional 12V Car Adapter
- MS-DOS V6.0 and MS-Windows V3.1 standard

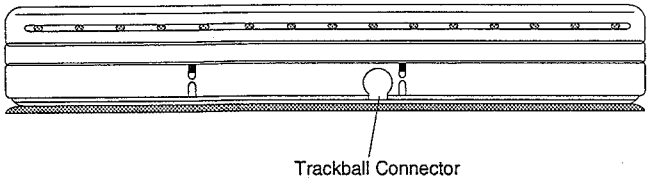
1-4. System Configuration



2. External View

(1) The Front Panel

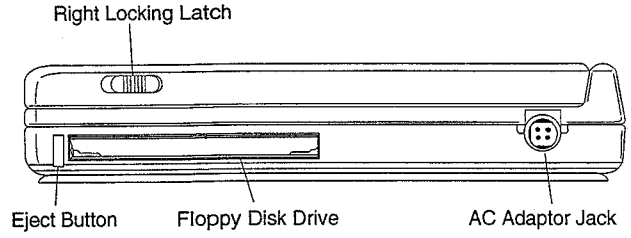
Located in the front panel is the external trackball port (PS/2 connector) and the support holes to secure the device. Only the optional trackball can be connected to this port.



(2) The Right Panel

The system's floppy disk drive, the AC adaptor jack and the right locking latch can be found on the right side of the case.

Floppy Disk Drive



Located in the front part of the right panel, the drive is easily accessed when the machine is in use. The drive is a standard 3.5" format design which can read and write to 1.44MB (2HD) and 720KB (2DD) capacity diskettes.
When a 3.5" diskette is inserted in the drive slot, it will slide into the drive and give an audible click when fully inserted. The eject button beside the slot will pop outwards a little. When you wish to remove the diskette, simply press the eject button and the diskette will eject to allow you to slide it out of the drive.

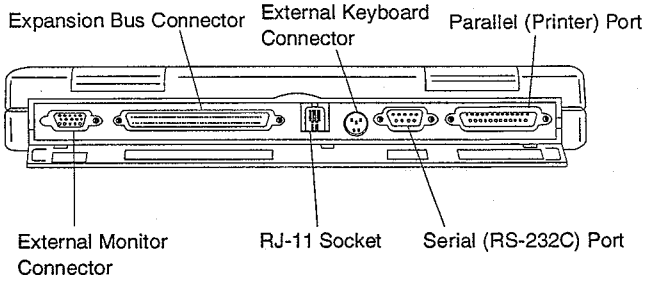
AC Adaptor Jack

This 4-pin socket is the power input port for the AC adaptor. The AC adaptor converts local AC power (110V or 240V) into a DC supply for use by the system. The AC power supply is used to power the system and also to recharge the battery

Right Locking Latch

You need to push this along with the left screen latch on the left panel towards you to open up the system.

(3) The Rear Panel



The rear panel of the system is a compartment containing various ports of the system. The compartment cover is hinged but is also completely removable by pulling it away from its hinges. There is a finger slot at the top. With a finger, flip open this slot to open the compartment cover. The expansion bus connector has a special sliding door. It has a door slot that you can use to slide the door open. You will only need to open this door when linking to an optional port replicator or to any third party device.
The illustration below shows the ports that are available in the compartments.

External Monitor Connector

The external monitor connector is a 15-pin female D-SUB connector used to connect the system to an external analog VGA monitor. When being used as a "desktop" machine, you can enjoy the full power of the system's VGA graphics capability by connecting a monitor through this port.
The system's VGA controller also supports simultaneous display output on the system's LCD and on an external monitor connected to the system. The controller can allow up to a maximum of 1024x768x16 color resolution when displaying on an external monitor.

Expansion Bus Connector

The 200-pin expansion bus connector is provided for connection to an optional port replicator.

RJ-11 Socket

This socket is the telephone cable input port for the installation of an internal fax/modem.

External Keyboard/Keypad Connector

The 6-pin mini-DIN connector can be used by a full-sized PS/2 keyboard. When a full-sized keyboard is connected to this port, the system's own keyboard remains active.
A PS/2 mouse can also use the mini-DIN port provided that the optional keyboard/mouse adaptor is first inserted in the mini-DIN connector. This adaptor reassigns the pinout from the PS/2 mouse so that it can be used by the mini-DIN connector. The adaptor also provides a keyboard connector so that a PS/2 mouse and PS/2 keyboard can both operate through the mini-DIN port.

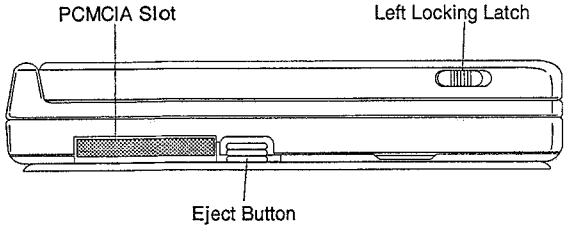
Serial (RS-232C) Port

The system has a standard 9-pin male D-SUB connector. This connector allows the system to connect to peripheral devices which use serial communications. The serial port of the system is identified as COM1.

Parallel (Printer) Port

The parallel port is a D-SUB 25-pin female connector which connects the system to devices which use parallel communications. Usually, this port will be used by a parallel printer.
This port can also be used by an external 5.25-inch floppy disk drive. The port can only perform one function, either as a parallel port or an external floppy disk drive port. The Setup utility allows you to choose the state of this connector. Parallel device connected to the system's parallel port are identified as being located at LPT1.

(4) The Left Panel



The left panel's main feature is the PCMCIA Type II drive.

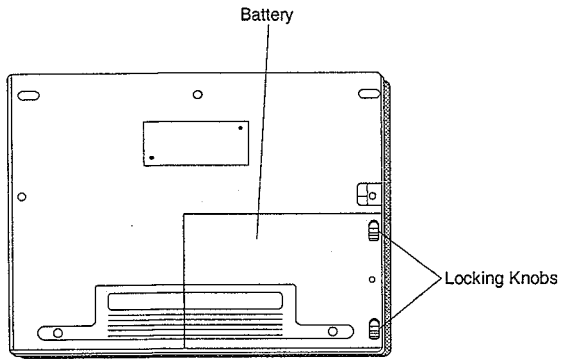
PCMCIA Drive

This slot is a standard PCMCIA Type II drive and will accept Type I and Type II PC cards. You can easily access this slot when the machine is in use.

Left Locking Latch

You need to push this along with the right screen latch on the right panel towards you to open up the system.

(5) The Bottom Panel



Battery Compartment

The battery is located at the bottom of the system. It has two locking knobs to secure it in the compartment.
The Ni-MH battery is enclosed in a plastic package for insertion into the battery compartment. To remove the battery, pull the locking knobs inward and use the fingernail slot on the right center of the battery to lift it out of the battery compartment.

3. Internal View

(1) LCD Screen

By pushing the screen backwards, you can set the angle of the screen however you wish for a good viewing position.
One small Cold Cathode Flourescent Tube (CCFT) is used to backlight the PC-7850 system display. Two small CCFTs are used to backlight the PC-8150 and PC-8650 system displays. The brightness control is located to the right of the LCD screen. Careful adjustment of the switch obtains optimum clarity.
To save battery power, the system has a feature that powers down the LCD backlighting when it has not been used for a specified amount of time.

Monochrome LCD Screen (PC-7850)

The system's 9.6" screen uses a paper-white Liquid Crystal Display (LCD). It has a response time of 150ms which means you can comfortably use a mouse with the system and the screen pointer doesn't disappear when the mouse is moved quickly.
The system has an onboard VGA graphics chipset supported by 512 KB of video RAM. It provides up to 64 levels of gray scale and exceptional clarity on the 640 x 480 pixel screen. Up to 1024 x 768 x 16 color resolution can be reached when displaying using an external monitor.

Color STN Screen (PC-8150)

The system's 9.6 STN (Supertwist Nematic) screen uses a passive color matrix screen LCD. Dual-scan display is supported allowing faster graphics redrawing response time. Simultaneously, 256 colors can be displayed.
The system has an onboard VGA graphics chipset with 512 KB of video memory. The built-in LCD is a 640 x 480 pixel screen and up to 1024 x 768 x 16 colors resolution can be reached when displaying using an external monitor.

TFT LCD Screen (PC-8650)

The system's 8.4" screen uses a vibrant active matrix TFT (Thin Film Transistor) LCD. This LCD screen has a fast response time which means you can comfortably use a mouse with the system and the screen pointer doesn't disappear when the mouse is moved quickly across the screen. The LCD screen is fixed at a very high contrast level producing graphics with clear and vivid colors. Simultaneously, 256 vibrant colors can be displayed.
The system has an onboard VGA graphics chipset with 512MB video memory. The built-in LCD is a 640 x 480 pixel screen and up to 1024 x 768 x 16 resolution can be reached when displaying using an external monitor.

(2) Indicator Panel

The indicator panel uses a Liquid Crystal Display to indicate your computer's current mode or status. The icons are visible when a mode or feature is active. The first three icons indicate the keyboard modes—Caps Lock, Num Lock and Scroll Lock. When the Num Lock is visible, the numeric keypad embedded in the alphanumeric keys of the keyboard is active. The rest represent the features of the system.

A This icon is visible when the keyboard is in Caps mode.

1 This icon is visible when the keyboard is in Num Lock mode.

This icon is visible when the keyboard is in Scroll Lock mode.

This icon is visible when the computer is in Suspend mode.

This icon is visible when the internal fax/modem is receiving or transmitting data.

This icon is visible when the computer is accessing the hard disk.

This icon is visible when the computer is accessing the floppy disk.

This icon is visible when the computer is powered by the Ni-MH (Nickel Metal Hydride) battery. The battery icon will start flashing when there is only a few minutes of battery power left.

This icon is visible when the computer is powered by the AC adapter.

(3) Screen Controls

Monochrome & STN Brightness and Contrast controls

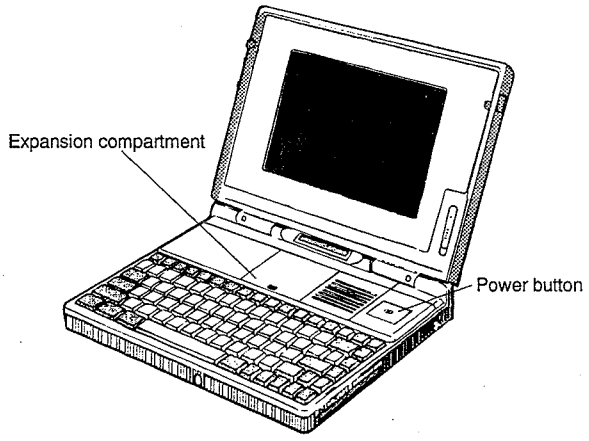
The two sliding switches just below and to the left of the LCD screen are the contrast and brightness controls for the LCD screen. These switches help you obtain the best possible screen display. The switches are quite sensitive and require careful positioning to obtain the best effect.
In the monochrome version (PC-7850) the lower switch is the contrast switch. It affects the bias voltage of the LCD screen itself. The upper switch is the brightness switch. It varies the intensity of screen backlighting. Sliding the switches to the right increases intensity, and sliding to the left decreases intensity.
In the color STN version (PC-8150), the sliding switches are also below the LCD screen and in-line with each other. The contrast switch is nearer the left edge of the system.

TFT Brightness Control

The TFT LCD screen has a very high contrast level so that the screen does not need contrast adjustment. There is however a brightness control sliding switch located to the right of the LCD screen. Sliding the switch upwards increases intensity and sliding downwards decreases intensity.

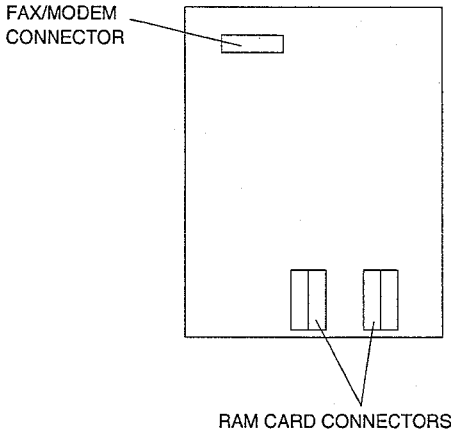
(4) Power switch

The power button, located to the right of the indicator panel and just above the keyboard turns the power ON or OFF. This button controls all the power to the system regardless of whether you are using a battery or an AC power supply. Press the power button to turn the power ON. Press the button again to turn the power OFF.



(5) Expansion Compartment

This compartment is located to the left of the power button. Removing the inside cover allows you to install the optional internal fax/modem, the optional RAM card and replace the system clock battery. The fax/modem exactly fits the inside cover space.



(6) Keyboard

The system's keyboard has 4 sections: Arrow keys, Function Keys, Typewriter Keys and the Numeric Keypad

Arrow (Cursor) Keys

The arrow keys at the lower right of the keyboard move the cursor. Pressing the arrow key moves the cursor one position in the direction of the arrow. Holding down an arrow key repeats the action.

Function Keys

How the function keys (F1-F12) operate depends on the program you run. Some of these keys perform special functions when you use them in combination with the Fn key.

Typewriter Keys

This main section of the keyboard is similar to a standard typewriter's keyboard. However, there are some non-standard keys on the computer. The following non-standard keys have special functions on the system.

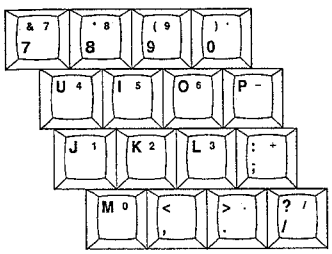
Ctrl Use the Ctrl (Control key) in combination with other keys to perform specific operations. To use a Ctrl key combination, hold down Ctrl while you press the other key(s).

Fn Use the Fn (Function key) in combination with certain keys to control special hardware functions. See "Special Keyboard Functions".

Alt Use the Alt (Alternate key) in combination with other keys to perform specific operations. To use an Alt key combination, hold down Alt while you press the other key(s).

Numeric Keypad Area

The keyboard's numeric keypad area is similar to a calculator keyboard. Press NumLock to use the keypad to enter numbers. When you press NumLock, the NumLock icon appears to show that the computer has activated the embedded keypad area instead of normal keyboard characters.



To enter one of the alphabet characters when you have turned on the keypad, hold down Fn (Function key) while you press the key of the character you want to enter.
To turn off the keypad area, press NumLock again and the Num Lock icon disappears.

Special Key Combinations

The system provides special key combinations to handle various functions.

Ctrl+Alt+Del

Halts all operation of your computer and commands it to reset.This is also called a "warm boot". The computer will halt all operation and will restart afresh. This key combination is useful if you encounter hardware or software problems which "lock up" your system.

Ctrl+Alt+S Opens up the system Setup utility

Fn+F4 Toggles the LCD display mode between Normal and Reverse. This applies to both text and graphics environments. Your display is in normal mode when the screen uses white characters on a black background. Reverse mode displays black characters on white background. (Only for PC-7850 model)

FN+F5 Toggles the display between the built-in LCD, the external monitor or both the built-in LCD and external monitor

Fn+F6 Toggles the LCD backlight between OFF and ON.

Fn+B This key combination disables the Battery Low beep. Note that this combination disables the beep temporarily but does not change the data in the Setup utility.

Spacebar Resumes the system from the Suspend mode. The system will return to exactly the same state as it was when Suspend mode was activated.

Fn+Esc This key combination opens up the system power management control in the Setup utility when in the DOS or Windows environment. The power managemnt control will allow you to setup the power management features of your system.

Ctrl+Alt+↑ Runs the CPU using Fast.

Ctrl+Alt+↓ Runs the CPU using Slow

Note that the Ctrl+Alt+↑ and Ctrl+Alt+↓ are not functional under Windows.

4. Software Specifications

4-1. The Setup Utility

The Setup utility program stores the configuration of your machine in CMOS memory where it is maintained by a small battery affixed to the system board. Each time you switch on the system, this stored information provides a reference point for the Power On Self Test (POST) and initialization routine. Therefore, whenever you make changes to your system, such as adding memory or installing an external floppy drive you should always run Setup to configure the new hardware in CMOS memory.
If the POST encounters any discrepancies between the Setup data and the actual system configuration, it will generate a message like this:

Invalid configuration information—Please run SETUP program.

Press the F1 key to continue, F2 to run setup utility

The Setup utility consists of two pages. The first page allows you to set up or modify the System Configuration parameters such as adding RAM, changing the CPU speed, attaching an external floppy disk and so on. The second page allows you to set the Power and Video configuration parameters.
When moving the cursor from one item to another, use the control arrow keys. To enter values for the selected item, use + or - keys. The + key moves forwards through the selection list while the - key moves backwards. Press Spacebar when there are only two choices in the item field to toggle between them, as for example, Enabled or Disabled. You may need to press some particular keys if a message appears requesting you to do so. Other available keys are displayed on the bottom of each screen.

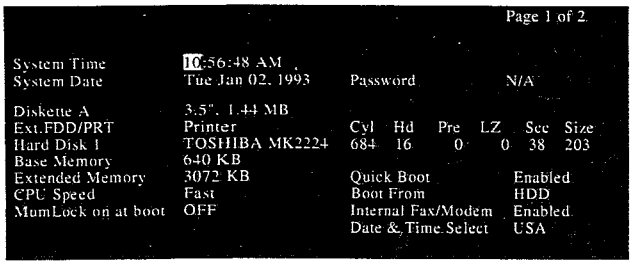
Page 1 - System Configuration

The first page of the Setup utility is the System Configuration screen. You can only enter this page when in DOS. Do not try to enter this utility when in an environment other than DOS. Also, be sure that all your application programs are closed before entering the System Configuration.
Open up the System Configuration page by pressing Ctrl+Alt+S. Press PgDn to turn to the Power and Video Configuration in page 2. To exit the Setup utility, first, you need to save the modified parameters and then re-boot your system to have all the changes take effect.

Page 2- Power and Video Configuration

There is no need to close any running application to make changes in the Power and Video Configuration screen of the Setup utility. Press Fn+Esc to open up this page of the Setup utility whether in DOS or in the Windows environment. To save and exit this screen page, you need not re-boot your system. Your changes will take effect immediately.
The Fn+Esc key combination will not allow you to view and modify the System Configuration.

4-2 Page 1 of Setup Screen



A screen similar to the one shown above is the System Configuration of the Setup utility. Your own machine will have a similar setup, though the different items may be different.

1. System Time/System Date

The system has a RealTime Clock/Calendar which is maintained by the onboard battery. If the date and time need changing, highlight the items and set the correct time and date. You cannot change the seconds item except to reset the counter to zero. The day of the week is automatically updated as you change the other items.

2. Diskette A

This item refers to the floppy disk drive installed in your system. The system's factory-installed floppy disk drive is of the 3.5" type, and has a 1.4 MB capacity.

3. Ext FDD/PRT

If you have an external floppy disk drive connected to your computer, select 5.25", 1.2 MB or 5.25", 360 KB according to the capacity of the drive. If you do not have an external drive, select PRT to configure the parallel port as a printer port.

4. Hard Disk 1

Hard disk 1 refers to the installed hard disk. This item selects the type of your hard disk. Many hard disk types are qualified for installation in your system.Your system Setup utility Hard Disk item is MK224FC as default.

5. Base Memory/Extended Memory

These items refer to the RAM you have available in your system. Under the MS-DOS the Base Memory takes up to a maximum of 640 KB. Extended memory is all memory above 1 MB. Base memory should always be set to 640 KB. The default setting of Extended memory is 3072 KB.
Note, however, that the sum of the Base and Extended memory is not equal to the total memory installed in your system. This is because some memory is used to copy the system BIOS and video BIOS for better performance.

6.CPU Speed

The system CPU can run at two different speeds, fast and slow. You should select fast option for maximum performance.
When you select fast, the CPU runs normally. If you select slow, the CPU reduces speed to a fourth of its original speed. You might wish to lower the system speed in order to play some computer games, or you might wish to prolong you battery life by a few minutes by setting this item to low.
You can also use key combinations without using the Setup utility to configure the system CPU to run fast or slow. Press Ctrl+Alt+↓ key combination to let the CPU run slow. Press Ctrl+Esc+↑ key combination to let the CPU run fast. These keystrokes are temporary and do not affect the Setup data. These key combinations do not work when in the Windows environment.

7. NumLock On at Boot

The NumLock setting, if set to ON, tells Setup to activate the NumLock mode when you re-start your system. In NumLock mode, the embedded numerical keys will become functional. Setting this item to OFF will deactivate the NumLock mode.

8. Password

When the Password setting is enabled, it tells Setup to activate the security password feature. A user specified password code of not more than 7 characters will protect the system from unauthorized access. At every system start up, a password prompt, asking you to enter your password code will appear. The system will start the POST routine only after you have entered the proper password.

Setting up the Password

1. Open up the System Configuration screen. Highlight the Password value item which shows N/A (Not Enabled) as the default value. You will see the following message:

   ```
   Warning! Changes to this field will alter
   your POST security code. Press ENTER to
   continue or any other key to exit without
   changes
   ```

2. Press Enter and the system will prompt the following message:

   ```
   You may now enter the new password
   directly if you would like to set it.
   ```

3. Key in a maximum of 7 alphanumeric characters as your password. A message prompting you to re-enter the password for verification will appear.

   ```
   Re-enter your correct password for
   verification.
   ```

4. Re-write the password. If it is exactly the same as the first entry, the system will prompt the following message and will replace the "N/A" to "Enabled".

   ```
   New password is now installed. Press any
   key to continue.
   ```

   If the second entry was different from the first, the system will prompt the following message:

   ```
   Verification of your NEW password was
   incorrect! The original password remains
   unchanged. Press any key to continue.
   ```

5. Start all over again. This time, be careful how you enter the password.

Change or Remove the Password

1. Open up the System Configuration screen and move the cursor arrow keys to the password item. Highlight "Enabled" and the system will prompt the following message.

   ```
   Warning! Changes to this field will alter
   your POST security code. Press ENTER to
   continue or any other key to exit without
   changes.
   ```

2. Press Enter if you wish to change the current password. The system prompts the following message after you press Enter.

   ```
   Enter the current security password for
   entry to this field.
   ```

3. Enter your current password. Then, the system will prompt the following message.

   ```
   Verification of the old password was
   correct. You may now enter the new
   password or type "/" to remove password
   security.
   ```

4. Enter the new password or type F1 to remove the password security. If you wish to change the password, follow steps 3, 4, 5 in the previous "Setting up the Password" section.

9. Quick Boot

The Quick boot setting allows you to select a faster way of restarting your system. You may enable this item if you wish to skip the hardware diagnostic sequence.

10. Boot From

This item refers to the source of the DOS system command that is loaded in the system during start up time. The system will look for the DOS system command either in the HDD, the FDD or the PCMCIA drive depending on the setting you have selected. You will normally set this to HDD where your DOS system command is stored. However, in some cases you may choose the other two drives for some special applications.

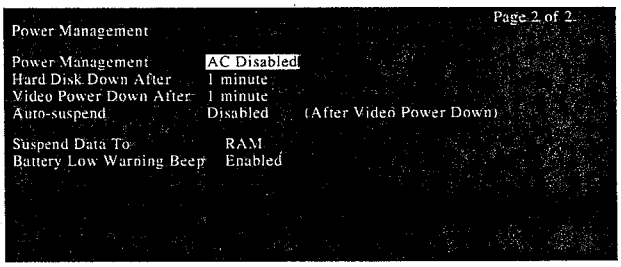
11. Internal Fax/modem

This setting tells your system whether to enable or disable the operation of an internal fax/modem. It has been set Enabled as default allowing you to have you fax/modem ready for data and fax immediately

12. Date & Time Select

This item specifies the format of the system Time and Date. If you select USA, the time is shown using a 12-hour clock followed by AM or PM and the date appears as Day-Month-Date-Year. If you select Europe, the time is shown using a 24-hour clock and the date appears as Day-Date-Month-Year.
One more page of the Setup utility, Power and Video utility can be accessed by pressing the PgDn or PgUp keys.

4-3 Page2 of Setup Screen



A screen similar to the one shown above is the Power and Video Configuration Screen of the Setup utility.

1. Power Management

Your system is installed with three user-controlled power management features. These powerdowns are implemented in the system and they work automatically. Possible settings are Enabled, AC Disabled and Disabled. Setting this item to Enabled activates all the powerdown features whether using the AC adapter or the Ni-MH battery. Selecting AC Disabled deactivates all the powerdowns when an AC adapter is attached to the system. Finally, selecting Disabled deactivates all the powerdowns whether using the AC adaptor or the Ni-MH battery.

2. Hard Disk Down After

If the hard disk is not accessed for a specified time, the hard disk will power down. When the hard disk is accessed, the drive will automatically be resupplied with power. Possible settings are Disabled and from 1 to 15 minutes.

3. Video Power Down After

If no keystroke or video activity takes place for the specified time, the LCD display will power down. Any keystroke will resume power to the LCD display. Possible settings are Disabled and from 1 to 16 minutes.

4. Auto-Suspend After

The Auto-Suspend timeout starts counting after the Video Power Down timeout elapses. The system will enter Suspend mode automatically when the Auto-suspend timeout elapses. All system components will power down except for the memory, the core logic chip, the VGA and PCMCIA controllers. To exit the Suspend mode, simply press Spacebard. The system will resume power to all the components that were powered down. Possible settings are Disabled and from 5 to 60 minutes.

5. Suspend Data to

This item allows you to choose whether to suspend your current data to RAM or to Disk when you enter the Suspend mode. Suspend to RAM is a power management feature that power's down almost all of the system's components to save power. Suspend to Disk however, is a handy feature implemented in your system that will facilitate your computer operations.
The system is set default as Suspend to RAM. When you suspend your computer, your data will be stored to RAM and the system will enter the Suspend mode. To exit the Suspend mode, press Spacebar. You will return to the application that was active before the system was suspended. You will use this feature when changing the nearly-discharged battery or when you have to pause your operations but plan to get back to it after some time.
You can also configure your system to Suspend to Disk. The system preserves all the current application programs in the memory as a file to a partitioned area in the hard disk. Then the computer turns off automatically. When you turn on the system, the computer will open up all those application programs saved and returns you exactly to the application program that was active before you suspended your data. Suspend to Disk is a useful feature incorporated in your system. While you can also use it when changing your battery, it is more of a special function for convenience. For example, when you are just about ready to turn off your computer after a day's work, you may want to utilize this function. Suspend to Disk loads your data and all opened Windows application programs to the hard disk and conveniently turns off the the system for you without you having to quit each application manually. The next time you turn on your system to continue your computer work, the system automatically opens up all those suspended-to-disk application programs from the partitioned area from where you left off. By then, you have just saved a lot of waiting time loading the application programs one by one.
To facilitate suspend to Disk, 9 MB of your hard disk space has been reserved. This means, youcan safely suspend to Disk with a 4 MB expansion memory card installed in your system. All applications in the memory will be stored in the hard disk without lacking disk space.

6. Battery Low Warning Beep

The system buzzer is programmed to beep intermittently when the system estimates that there are only a few minutes of Ni-MH battery power left. You can enable or disable this function using this item.
Using the Fn+B key combination will also disable the system buzzer. However, this keystroke will not affect the Setup data.

7. Display (Text Mode and Graphics Mode)

Setting this item to Normal displays white characters on a black background in both text and graphics modes. To reverse the screen and display black characters on a white background, select Reverse.
You can also change the display mode by using the VGA utility. Note that these operations only change the display mode and not the Setup data. Also, this feature in only works in PC-7850 monochrome systems.

5. System Power Management

The system power management includes a processor powerdown, three system powerdowns, the Suspend and Cover close modes and a low power alarm. The operation of the power management depends on the power management setting you have selected in the Setup utility.
Your system uses the SL-Enhanced 486DX processor with a built-in static design to use the CPU only when needed. This powerdown is automatic and transparent. It is not included in the Setup utility and you will not detect it when in operation. Whenever the computer is unused for about 4 seconds, the processor will slow down to 2 megahertz. As soon as the computer becomes active again, the processor will instantaneously return to its full clock speed.

1. Suspend Mode

The Suspend mode feature in your system reduces power consumption. Your system has the "Suspend Data to" item set to RAM as default. But you may choose to set it to Suspend Data to Disk.
If you are displaying to an external monitor using CRT mode only at a high resolution of 1024 x 768 or 800 x 600 resolution, the Suspend mode is non-functional. If you are displaying to an external monitor using 640 x 480 resolution, the Suspend mode is functional.
If the modem receives an incoming call while the system is suspended, the system will power up all the system components in order to receive the call according to the automatic answering instructions of your modem software.

Suspending to RAM

Your system will enter the Suspend mode in four different ways:

1. You have pressed the Fn+S key combination
2. The time specified in the Auto Suspend field in the Setup utility has elapsed without any activity on the keyboard, trackball, video buffer, or modem port.
3. You have closed the screen assembly cover of the computer and you are not displaying to an external monitor
4. Your battery power is critically low and you did not respond to the low battery power signals that the system emmitted and the system still remained power on. the system will automatically enter the Suspend mode about one minute after the system low power buzzer sounds.

In the first three Suspend methods, resume power to the computer by pressing the Space Bar. Immediately connect an AC adapter to the system or install a charged battery to the computer before turning on the system that entered Suspend mode due to low battery power if the "Suspend Data To" item is set to RAM. Do this as soon as possible so as not to use up all the battery power in the tiny battery maintaining the data in system memory.

Suspending To Disk

You can only choose to suspend to disk if you have set a partitioned hard disk space in which to suspend all your data. The Space Bar key will not resume the system's power, instead you must use the power switch to restart your computer. After it has restarted, it will use the disk image to recreate the state of your computer before you implemented the Suspend to disk..

2. Cover-Close Mode

When the system cover is closed without power being switched off, it will beep once and go into Suspend mode. To resume power to the system, open the cover and press the Spacebar to leave the Suspend mode. If you have set your system to Suspend to RAM, the above-mentioned power management feature takes place. If you have set your system to Suspend to Disk, Cover-close will suspend all your data to disk and turn off the computer. When you turn on your computer, your computer will be returned to the same application that was opened before you activated the Cover-close mode.
If you are displaying to an external monitor only, or to both the built-in LCD and an external monitor, closing the cover will not suspend the system. The computer will continue sending the VGA signal to the external monitor when in CRT mode. When using both the built-in LCD and an external monitor, Cover-close mode will only cut off power to the built-in LCD but will continue sending the VGA signal to the external monitor. Opening the cover will resume power to the built-in LCD.

3. Powerdowns

Your system is equipped with three powerdowns. these powerdowns represent different types of power saving modes. They allow you to set timeouts to powerdown the LCD, the hard disk and other system components.

Hard Disk Powerdown

The hard disk powers down if a user specified time (1-15 minutes) elapses with no hard disk access. When the hard disk is accessed, it will resume power. If the system is displaying to an external monitor, the hard disk powerdown will still function.

Video Powerdown

The LCD powers down if there is no keystroke, or video activity for a user specified time (1-16 minutes). Any activity, a keystroke for example, will resume power to the LCD.

Auto-suspend timeout

The Auto-suspend timeout automatically sets the system to Suspend mode after the user specified time (5-60 minutes) has elapsed.
In non-DOS environments, e.g. Windows, OS/2, these power management routines may not be functional.

4. Advanced Power Management

The system supports advanced power management using the MS-DOS device driver POWER.EXE. This driver should be loaded by the CONFIG.SYS file on system start up by writing the line

```
DEVICE.=C:\POWER.EXE
```

into the file. If you are using the AC adapter, you can prevent the driver from being loaded by placing REM in front of the command:

```
REM DEVICE=C:\POWER.EXE
```

6. Power On Testing

The following terms are used in the Power On Testing table:

Pattern Test

One or more particular patterns are written to a location then read back from the same location. Examples of patterns used are 55h and AAh. If the value read does not match the value written, the test is considered a failure.

Rolling Ones Test

Several patterns are constructed. These patterns re[resent a one rolling through the given location. For example, to roll a one through three bits, the following patterns would be constructed: 001, 010, 011, 100, 101, 110, and 111. The patterns are written to the location and then read back, one by one. If the value read does not match the value written, the test is considered a failure.

Checksum Test

All of the values in a given range of locations are added together. The range includes a location which, when added to the sum of the ranges, will produce a known result, such as zero (0).

Beep Codes for System Errors

Beep Code	Diagnostic Code	Description	Test Performed
None	01h	CPU register test in progress or failure	Pattern test of most of the 16-bit CPU registers. Failure will result in a system halt.
1-1-3	02h	CMOS write/read test in progress or failure.	Rolling ones test in the shutdown byte (offset 0Eh) of the CMOS RAM. Failure will result in a system halt.
1-1-4	03h	ROM BIOS checksum test is in progress or failure.	The range of ROM that includes the BIOS is checksummed. Failure will result in a system halt.
1-2-1	04h	Programmable interval timer 0 test in progress or failure	Over a period of time, the current count values in timer 0 are read and accumulated by ORing them into the values read so far. It is expected that during the time period, all bits will be set. Failure will result in a system halt.
1-2-2	05h	DMA channel 0 address and count register test in progress or failure.	Rolling ones and rolling zeros test of the address and count registers of DMA channel 0. Failure will result in a system halt.
1-2-3	06h	DMA page register write/read test in progress or failure.	Pattern test of DMA page registers. Failure will result in a system halt.
1-3-1	08h	RAM refresh verification test in progress or failure.	Over a period of time, the refresh bit (bit 4) in port 60h is read and tested. The refresh bit should toggle from 0 to 1, then 1 to 0 within the time period. Failure will result in a system halt.
None	09h	First 64K RAM test in progress.	No specific test is performed — just indicates that the test is beginning (i.e., no failure).
1-3-3	0Ah	First 64K RAM chip or data line failure, multi-bit.	The first 64K of RAM is tested with a rolling ones test and pattern test. If any of the pattern tests fail, then the BIOS reports that multiple data bits failed (see specific bit tests following). Failure results in a system halt.
1-3-3	0Dh	Parity failure first 64K RAM.	At the completion of the rolling ones and pattern tests of the first 64K, the BIOS checks the parity error bits (bits 7 and 6) of port 60h. Failure results in a system halt.

Beep Code	Diagnostic Code	Description	Test Performed
2-1-1 2-1-2 2-1-3 2-1-4 2-2-1 2-2-2 2-2-3 2-2-4 2-3-1 2-3-2 2-3-3 2-3-4 2-4-1 2-4-2 2-4-3 2-4-4	10h-1Fh	First 64K RAM chip or data line failure on bit x (see test description).	The first 64K of RAM is tested with a rolling ones test and a pattern test. If any of the rolling ones tests fail, then the BIOS reports the specific bit that failed. To determine the bit number from the diagnostic code, subtract 10h. For example, if 15h is displayed at the diagnostic port, bit 5 failed. Failure results in a system halt.
3-3-1	20h	Slave DMA register test in progress or failure.	Pattern test of channels 1 through 3 of the slave controller (starting port address = 2). Failure results in a system halt.
3-1-2	21h	Master DMA register test in progress or failure.	Pattern test of channels 1 through 3 of the master DMA controller (starting port address = C4h). Failure results in a system halt.
3-1-3	22h	Master interrupt mask register test in progress or failure.	Rolling ones and zeros tests of the mask register of the master programmable interrupt controller (port 21h). Failure results in a system halt.
3-1-4	23h	Slave interrupt mask register test in progress or failure.	Rolling ones and zeros tests of the mask register of the slave programmable interrupt controller (port A1h). Failure results in a system halt.
None	25h	Interrupt vector loading in progress.	No specific test is performed — just indicates that the Interrupt Vector table is being initialized (i.e., no failure).
3-2-4	27h	Keyboard controller test in progress or failure.	The self-test command (AAh) is issued to the 8042 (keyboard controller) and the results are monitored. Failure results in a system halt.
None	28h	CMOS RAM power failure and checksum calculation test in progress.	The power-fail bit in CMOS RAM is tested and the lower CMOS RAM area is being checksummed. A failure does not result in a system halt.
None	29h	CMOS RAM configuration validation for video in progress.	No specific test is performed — just indicates that the configuration specified in CMOS for video is being matched against the actual installation. A failure does not result in a system halt.
3-3-4	2Bh	Screen memory test in progress or failure.	The video buffers (B0000h and B8000h) are tested with a pattern test and a rolling ones test. Failure will result in a beep code but not a system halt.
3-4-1	2Ch	Screen initialization in progress.	Until the video installation is confirmed, any calls to INT 10h Function 0 (set mode) will be prefaced with this diagnostic code. There is no expected failure from this.
None	2Eh	Search for video ROM in progress.	No specific test is performed by the system BIOS — just indicates that the BIOS is about to jump to the initialization code in the video option ROM.
None	30h	Screen running with video ROM.	No specific test is performed — just indicates that a video option ROM was found and is believed to be operating.
None	31h	Monochrome monitor operable	No specific test is performed — just indicates that the BIOS believes a monochrome monitor is installed and is operating.
None	32h	Color monitor (40 column) operable	No specific test is performed — just indicates that the BIOS believes a color monitor is installed and is operating. The mode has been set to 40-column as selected by the user in CMOS RAM.
None	33h	Color Monitor (80-column) operable	No specific test is performed — just indicates that the BIOS believes a color monitor is installed and is operating. The mode has been set to 80-column as selected by the user in CMOS RAM.
4-2-1	34h	Timer-tick interrupt test in progress or failure.	All interrupts except the timer-tick interrupt are masked off at the interrupt controllers. If a timer-tick interrupt does not occur during a specific timer period, an error message is displayed on the screen. The system does not halt.
4-2-2	35h	Shutdown test in progress or failure.	A return address is stored in 40:67h and the processor is reset via the keyboard controller. If a timer-tick occurs during this time period, an error message is displayed on the screen. Other failures are hard to detect. If possible, the BIOS will continue with POST, skipping the memory tests.
4-2-3	36h	Gate A20 failure.	To test exteded memory, the processor must be placed in protected mode and the A20 line must be enabled. For the memory tests, the BIOS generally uses the keyboard controller to enable A20. If the A20 line is not properly set during the memory tests, an error message is displayed on the screen and the memory tests are suspended. The system does not halt.
4-2-4	37h	Unexpected interrupt in protected mode.	During the memory tests, the processor is placed in protected mode. All interrupts in the interrupt descriptor table are initialized to point to a special handler that displays a message on the screen. All hardware interrupts are masked off and interrupts are disabled. The system does not halt when such an unexpected interrupt occurs.
4-3-1	38h	RAM test of memory above 64K in progress or failure.	The memory above the first 64K is tested with a rolling ones test and a pattern test. All success and failure messages are displayed on the screen and POST will continue.
4-3-2	3Ah	Programmable interval timer channel 2 test in progress or failure.	Over a period of time, the current count values in timer 2 are read and accumulated bu ORing them into the values read so far. It is expected that during the time period, all bits will be set. If an error is detected, an error message will be displayed on the screen and POST will continue.
4-3-4	3Bh	Real-time clock test in progress or failure.	Over a period of time, the Update-In-Progress bit of Status register A of the real-time clock is read and tested. The bit should toggle from 0 to 1 within the time period.
4-4-1	3Ch	Serial port test in progress or failure.	Pattern test of one or more of the installed serial ports. If a failure is detected, an error message will be displayed and POST will continue.
4-4-2	3Dh	Parallel port test in progress or failure.	Rolling ones test is done to one or more of the installed parallel ports. If a failure is detected, an error message will be displayed and POST will continue.
4-4-3	3Eh	Math coprocessor test in progress or failure.	An integer load and store is performed with the math coprocessor. If the values do not match, an error message will be displayed and POST will continue.

7. Bios Messages

The Power On Self Test (POST) is the system test and component initialization process performed by the ROM BIOS in the computer. The central hardware is tested and initialized first.
Proper functioning of the central hardware is required before further system tests can be run. In general, a failure in a test of the system board or its components will sound a beep, and halt the system. A failure in add-on boards or memory is reported on the screen.
There are two types of messages POST displays:

- Error messages indicating a failure in either the hardware, software or firm ware.
- Informational messages about the power-on and booting processes.

POST messages are listed below, with possible causes and solutions.
Messages which do not appear in this list indicate hardware faults which can only be rectified by internal checks.

POST Error Messages

```
Diskette drive (x) failure
```

Possible cause The floppy disk drive has failed.

Solution Run the diagnostics program to check the floppy disk drive.

```
Diskette read failure
```

Possible cause The diskette is either not formatted or defective.

Solution Replace with a formatted diskette.

```
Fixed disk configuration error
```

Possible cause The setting of Hard Disk in the Setup utility is wrong.

Solution Run the Setup utility and enter the correct values.

```
Fixed disk failure
```

```
Fixed disk controller failure
```

Solution Reboot. If this does not work, run the diagnostics program to check the hard disk drive.

```
Fixed disk read failure
```

Possible cause The hard disk is defective.

Solution Reboot. If this does not work, run the diagnostics program to check the hard disk.

```
Gate A20 failure
```

Possible cause The system board is defective.

```
Invalid configuration information - please
run SETUP program
```

Possible causes
Memory size is incorrectly configured.
Incorrect number of hard disk.

Solution Check the settings in the Setup utility.

```
I/O card parity interrupt at xx
```

Possible cause The system board is defective.

Solution Reboot.

```
Keyboard clock/data line failure
```

Possible cause The keyboard data line is defective.

```
Keyboard failure
```

```
Keyboard controller failure
```

Solution Reboot. If this does not work, run the diagnostics program to check the keyboard.

```
Keyboard stuck key failure
```

Possible cause One or more keys were pressed during the power-on self test.

Solution Avoid pressing any keys during the power-on self test except the **Space Bar** to terminate the memory test.

```
No boot device available
```

Possible cause Either the hard disk drive, the floppy disk drive, the diskette itself, the PCMCIA slot, or the IC card itself is defective.

Solution Reboot. If this does not work, replace with a bootable diskette or IC card. If you suspect the hard disk is faulty, run the diagnostics program.

```
No boot sector on fixed disk
```

Possible cause The hard disk is not formatted.

Solution Format the hard disk. Remember this wil erase the contents of the hard disk.

```
Non-System disk or disk error
```

```
Replace and press any key when ready
```

Possible cause The diskette in the floppy disk drive or the IC card in the PCMCIA slot is not formatted as a bootable diskette or IC card.

Solution Remove the diskette or the IC card, or replace with a bootable diskette or IC card and press any key.

```
Not a boot diskette
```

Possible cause The diskette in the floppy disk drive or the IC card in the PCMCIA slot is not formatted as a bootable diskette or IC card.

Solution Remove the diskette or the IC card and reboot.

```
Time-of-day not set - run SETUP utility
```

Possible cause The RTC time-of-day clock chip has failed.

Solution Reset the time and date in the Setup utility.

POST Informational Messages

```
XXX Conventional Memory, XXXXXK Extended
```

Meaning This message indicates the amount of memory that has tested successfully.

```
Memory tests terminated by keystroke
```

Meaning This message indicates that you have pressed the **Space Bar** while the memory tests were running. This stops the memory tests.

```
Press F1 to retry boot, F2 for SETUP
utility
```

Meaning This message indicates that an error was found during the power-on tests. Pressing **F1** allows the system to attempt to boot, and pressing **F2** brings you to the setup utility.

```
Press the F1 key to continue, F2 to run
the SETUP utility
```

Meaning This message indicates that an error was found during the power-on tests. Pressing **F1** allows you to start the system, ignoring the error, and pressing **F2** brings you to the setup utility.
You should press **F2** and enter the Setup utility.

CHAPTER 2. SPECIFICATION

1. HARDWARE

CPU: Intel SL-Enhanced 486DX-33 MHz
- With internal 8 KB cache memory
- With internal math coprocessor

ROM: 128 KB 200ns bootable EPROM
- Includes system BIOS and VGA BIOS
- Supports shadow BIOS RAM feature
- Supports shadow VGA BIOS feature

RAM: 4 MB RAM standard
- Onboard system 4 MB RAM (1M x 4 DRAM x 8 pcs, 70ns)
- 640 KB for conventional, 3072 for Extended memory
- Can be upgraded to 8 MB or 20 MB by installing optional 4 MB or 16 MB memory card (1M x 4 x 8pcs or 4M x 4 x 8pcs)
- Bus width:32-bit
- 1 wait state
- Page mode addressing
- Detects system RAM size automatically

DATA STORAGE:

2.5 inch 200 MB Hard Disk Drive
- Average access time:under 20ms

3.5 inch 1.44 MB / 720 KB Floppy Disk Drive

Optional external 5.25 inch 360 KB/1.2 MB Floppy Disk Drive
- shares the parallel port
- Configured and setup by software

DISPLAY: Monochrome STN-LCD with CCFT backlight
- Resolution:640 x 480 dots
- Standby and suspend mode feature
- 64 gray scales
- Viewing area:196mm (W) x 147.6mm (H)
- Dot pitch: 0.03mm
- LCD contrast and backlight brightness are adjustable by each volume
- Response time: typical 150ms
- Contrast ratio:18:1

Color STN-LCD with CCFT backlight
- Resolution:640 x 480 dots
- Standby and suspend mode feature
- 256 simultaneous colors
- Viewing area: 195mm (W) x 147mm (W)
- Dot pitch: 0.025mm
- LCD contrast and backlight brightness are adjustable by each volume
- Response time: typical 300ms
- Contrast ratio: 18:1

Color TFT-LCD with CCFT backlight
- Resolution:640 x 480 dots
- Standby and suspend mode feature
- vibrant 256 simultaneous colors
- Viewing area: 170.9mm (W) x 129.6mm (H)
- LCD backlight brightness is adjustable volume
- Response time: typical 55ms
- Contrast ratio: 50:1

Video Controller in Monochrome and Color STN
- VGA compatible
- On board 512 KB video memory
- Supports external VGA monitor up to 1024 x 768 x 16 resolution in CRT mode
- Simultaneous CRT and LCD display in 640 x 480 resolution

Video Controller in Color TFT
- VGA compatible
- On board 512 MB video memory
- Supports external VGA monitor up to 1024 x 768 x 16 resolution in CRT mode
- Simultaneous CRT and LCD display in 640 x 480 resolution

KEYBOARD:

IBM 101/102 like keyboard layout
- 85 keys (US layout)
- 86 keys (UK/German layout)
- Minimum 2.5mm key travel
- 12 programmable full-size function keys
- Fn key for special functions
- Inverted "T" cursor keys layout

INTERFACE:

PCMCIA connectors for PC Cards
- 68-pin connectors

VGA port for external analog VGA CRT monitor x 1
- D-sub 15-pin female connector

Expansion bus x 1
- 200-pin connector

RJ-11 standard phone jack for optional internal fax/modem

External keyboard/mouse x 1
- 6-pin mini-DIN connector
- Shared by PS/2 keyboard and PS/2 mouse
- for PS/2 mouse, need an adaptor

Serial (RS-232C) x 1
- D-sub 9-pin male connector
- 50-9600bps

Parallel (Centronics)/ FDD x 1
- D-sub 25-pin female connector
- Shared by printer and FDD

POWER SUPPLY:

Ni-MH battery
- 30.24W removable and rechargable Ni-MH battery pack
- 12 cells of 1700mAh AE-size Ni-MH battery
- Quick charging:1A contant charging current which can be fully charged within 2.2 hours
- Trickle charging: 60mA constant charging current which maintains battery fully charged

AC adapter
- Input: 110-240V±10% 50/60 Hz AC input
- Output: 21.6V DC
- AC cord is detachable from AC adapter
- Supports both Ni-MH and Ni-Cd battery.

BATTERY LIFE:

Only With Internal Battery: Minimum 3 Hours At PC Benchmark Test Rundown 2.0

LOW BATTERY ALARM:

Approx. 5 minutes before system shutdown: Battery icon flashes

Approx. 2 minutes before system shut down: Beeper sounds

POWER SAVE FUNCTION:

CPU

- static-design
- SMI (System Management Interrupt) for advanced power management
- Standby mode disable cache memory

Hard disk drive

- Spindle motor off
- Timeout parameter

Floppy Disk Drive

- Automatic power management

Cover Close alarm

- The system will beep twice and then enters the Suspend mode when the cover is closed.
- The system can wake up automatically when Space bar is pressed.
- System resumes power from Suspend mode by fax/modem ring.

CHARGING INDICATOR:

AC adapter

- Turns on while the battery is being charged and turns off when battery is fully charged

POWER CONSUMPTION

Typical 13.7W (PC-7850)
Typical 18.6W (PC-8150)
Typical 19.1W (PC-8650)

2. MECHANICAL

CONNECTORS:

External connectors for

Serial interface	:D-sub 9-pin connector
External CRT interface	:D-sub 15-pin connector
Expansion bus	:200-pin connector
PS/2 Keyboard/Mouse interface	:Mini-DIN 6-pin connector
Serial interface	:D-sub 9-pin connector
Parallel interface	:D-sub 25-pin connector
PS/2 Trackball	:Mini-DIN 6-pin connector

SWITCHES:

Power Switch (Press switch)

VOLUMES:

LCD contrast adjust volume (slide lever)
LCD brightness adjust volume (slide lever)

INDICATORS:

Battery icon
AC adapter icon
FDD icon
HDD icon
Fax/Modem icon
Caps Lock icon
Num Lock icon
Scroll Lock icon

DIMENSIONS:

PC-7850 :

- 11.42: (W) x 8.86" (D) x 1.65" (H)
- 290mm (W) x 225mm (D) x 42mm (H)

PC-8150/8650:

- 11.42: (W) x 8.86" (D) x 1.73" (H)
- 290mm (W) x 225mm (D) x 44mm (H)

WEIGHT:

- PC-7850: Approx. 5.5 Lbs. (2.5 Kg.)
- PC-8150/8650: Approx.6.4 Lbs. (2.9 Kg.)

3. SOFTWARE

OPERATING SYSTEM:

MS-DOS 6.0

- With DOS User's Manual
- Pre-installed in hard disk drive
- Also supplied on diskettes

MS-Windows 3.1

- With Windows 3.1 user's manual
- Pre-installed in hard disk drive
- Also supplied on diskettes

UTILITIES:

The following software programs are pre-installed in the hard disk drive and supplied by diskettes.

- High resolution driver (Video utilities) software
- Mouse driver software
- PCMCIA Socket Service
- PCMCIA Card Service
- PCMCIA I/O and memory card driver utility programs

4. OPERATIONAL AND STORAGE RANGE:

OPERATIONAL RANGE:

10° to 38°C (50° to 100°F)
10 to 80% humidity (non-condensing)

STORAGE RANGE:

-20° to 60°C (-4° to 140°F)

SHOCK RESISTANCE:

Operating	: 5 G
Non-operating	: 60 G

VIBRATION:

Operating	:5 ~ 200 Hz (5 G peak to peak)
Non-operating	:5 ~ 200 Hz (5 G peak to peak)

5. OPTIONS:

- 4 MB memory card (CE-771B)
- 16 MB memory card (CE-772B)
- Fax/modem card (CE-781M)
  14400bps MNP5/V42bis data modem with 14400bps send/receive fax
- Extra internal Ni-Cd battery (CE-771EB)
- Extra internal Ni-MH battery (CE-772EB)
- External Trackball (CE-781T)
- I/O (Input/Output) Port Replicator (CE-781PR)
- Car adapter (CE-771CA)
- Keyboard / mouse adapter (CE-771KA)

CHAPTER 3. DISASSEMBLY AND ASSEMBLY INSTRUCTIONS

1. Precautions

Before disasssembly, remove the AC adaptor and the built-in Nickel Metal Hydride battery.
Some components are very small so use a tidy worktable and store removed screws carefully.

2. Remove the Keyboard

1. Turn the unit upside down and place it on a soft mat.
2. Remove the rubber plugs and embedded screws.
3. Turn the unit back over and open up the screen cover. Open the inner and outer expansion compartments.
4. Remove the rubber plugs and embedded screws.
5. Remove the plastic panel which runs along the top of the keyboard and secures it in place.
6. Remove the two remaining screws which hold the keyboard in place.
7. Slide the keyboard free from the base of the unit and rasise it a few millimetres. Locate the two ribbon cables from the keyboard which are locked into connectors on the motherboard. Pull upwards on the motherboard connectors to unlock the cables, and slide the cables free from the connectors.
8. The keyboard can be completely removed.

3. Removing the Hard Disk Drive

1. Carry out steps 1 to 5 of the keyboard removal instructions.
2. Remove the single screw A which secures the hard disk drive in place.
3. Slide the hard disk drive to the left edge of the computer to free the drive from the vertical IDE drive interface.
4. Remove the hard disk drive entirely.

4. Remove the Upper Cover and Screen Assembly

1. Turn the unit over and raise the outer edge of the rubber feet, and remove the embedded screws underneath the feet.illust.
2. Remove the rubber plugs and embedded screws.
3. Turn the unit back over and open up the screen cover. Open the inner and outer expansion compartments.
4. Remove the rubber plugs and embedded screws.
5. Remove the plastic panel which runs along the top of the keyboard and secures it in place.
6. Remove the two remaining screws which hold the keyboard in place.
7. Slide the keyboard free from the base of the unit and rasise it a few millimetres. Locate the two ribbon cables from the keyboard which are locked into connectors on the motherboard. Pull upwards on the motherboard connectors to unlock the cables, and slide the cables free from the connectors.
8. The keyboard can be completely renoved.
9. Remove the single screw which secures the hard disk drive in place.
10. Slide the hard disk drive to the left edge of the computer to free the drive from the vertical IDE disk interface.
11. Remove the hard disk drive entirely.
12. Three wire harnesses connect the screen assembly to the motherboard. Disconnect the wire harnesses from the motherboard connectors.
13. Remove the upper cover and screen assembly from the base of the unit. The upper cover is secured to the base by some plastic snap fasteners on either edge of the computer. You can pull the upper cover free of the fasteners quite easily.
14. Remove the upper cover and screen assembly entirely.

5. Remove the Floppy Disk Drive.

1. Remove the upper cover and screen assembly as described above.
2. Locate the ribbon cable which connects the FDD to the motherboard.
3. Pull up on the motherboard FDD connector to unlock the FDD ribbon cable and slide the ribbon cable out of the connector.
4. Carefully slide the FDD out of the FDD compartment and remove it entirely.

6. Remove the System Motherboard

1. Remove the upper cover and screen assembly as described above.
2. Remove the FDD as described above.
3. Remove the screw A which secures the battery connector board to the base of the unit.
4. Pull upwards on the top edge of the battery connector board to disconnect the board from the motherboard connector.
5. Remove the two remaining screws B which secure the system motherboard to the base of the unit.
6. Carfully remove the motherboard from the base of the unit and remove it entirely.

7. Disassemble the Screen Assembly

1. Remove the upper cover and screen assembly as described above.
2. Carefully peel off the mylar frame which surrounds the LCD screen.
3. Remove the rubber plugs in each of the two screen hinges and remove the embedded screws underneath.
4. Remove the two screws in the upper right and left corners of the screen assembly.
5. Carefully remove the plastic screen cover from the screen assembly.
6. Disconnect the two cables from the upper edge of the inverter circuit board, and remove the three cables from the lower edge of the inverter circuit board. Remove the inverter circuit board from the screen assembly.
7. Remove the two screws in the lower left and right corners of the LCD panel which secure the panel to the screen assembly.
8. Lift the LCD panel out of the screen assembly. Disconnect the two wire harnesses from the left side of the LCD panel. You can then remove the LCD panel entirely.

Chapter 4. HARDWARE DESCRIPTION

1. General

1-1. BLOCK DIAGRAM

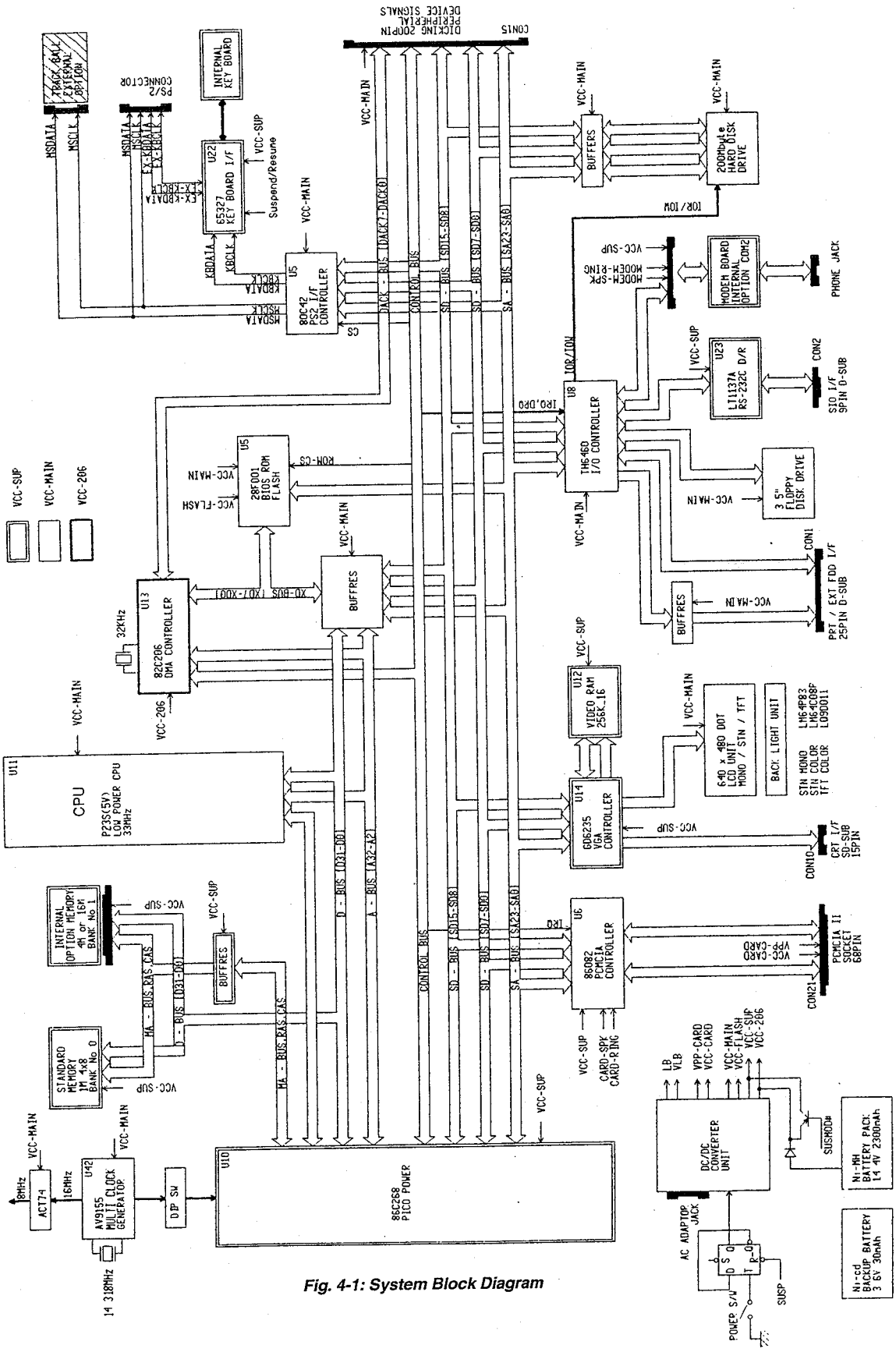
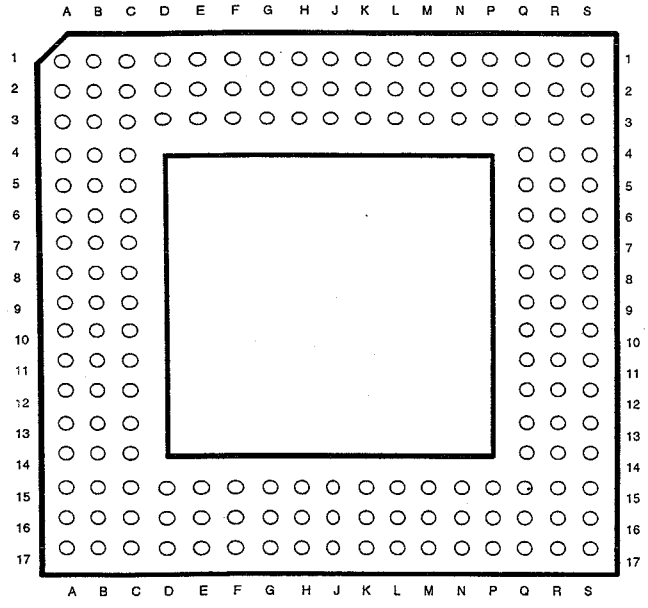


Fig. 4-1: System Block Diagram

2. Intel SL-Enhanced 486 DX CPU

(1) Package Diagram for 168 Lead PGA Package SL Enhanced Intel 486 DX



(2) Pin Cross Reference for 168 Lead PGA Package, SL Enhanced Intel486 DX

Address	Data	Control	NC	Vcc	Vss
A2 Q14	D0 P1	$\overline{A20M}$ D15	A12	A10(1)	A7
A3 R15	D1 N2	$\overline{ADS}$ S17	A13(2)	B7	A9
A4 S16	D2 N1	AHOLD A17	B12	B9	A11
A5 Q12	D3 H2	$\overline{BE0}$ K15	B13	B11	B3
A6 S15	D4 M3	$\overline{BE1}$ J16	C13	C4	B4
A7 Q13	D5 J2	$\overline{BE2}$ J15	R17	C5	B5
A8 R13	D6 L2	$\overline{BE3}$ F7	S4	E2	E1
A9 Q11	D7 L3	$\overline{BLAST}$ R16		E16	E17
A10 S13	D8 F2	$\overline{BOFF}$ D17		G2	G1
A11 R12	D9 D1	$\overline{BRDY}$ H15		G16	G17
A12 S7	D10 E3	BREQ Q15		H16	H1
A13 Q10	D11 C1	$\overline{BS8}$ D16		J1	H17
A14 S5	D12 G3	$\overline{BS16}$ C17		K2	K1
A15 R7	D13 D2	CLK C3		K16	K17
A16 Q9	D14 K3	$\overline{D/C}$ M15		L16	L1
A17 Q3	D15 F3	DPO N3		M2	L17
A18 R5	D16 J3	DP1 F1		M16	M1
A19 Q4	D17 D3	DP2 H3		P16	M17
A20 Q8	D18 C2	DP3 A5		R3	P17
A21 Q5	D19 B1	$\overline{EADS}$ B17		R6	Q2
A22 Q7	D20 A1	$\overline{FERR}$ C14		R8	R4
A23 S3	D21 B2	$\overline{FLUSH}$ C15		R9	S6
A24 Q6	D22 A2	HLDA P15		R10	S8

(3) Output Pins

The following table lists all the output pins, indicating their active level, and when they are floated.

Name	Active Level	When Floated
BREQ	HIGH	
HLDA	HIGH	
$\overline{BE3}$-$\overline{BE0}$	LOW	Bus Hold
PWT.PCD	HIGH	Bus Hold
$\overline{W/R}$, $\overline{M/IO}$, $\overline{D/C}$	N/A	Bus Hold
$\overline{LOCK}$	LOW	Bus Hold
$\overline{PLOCK}$	LOW	Bus Hold
$\overline{ADS}$	LOW	Bus Hold
$\overline{BLAST}$	LOW	Bus Hold
$\overline{PCHK}$	LOW	
$\overline{EFRR}$*	LOW	
A3-A2	N/A	Bus, Address Hold
$\overline{SMIACT}$	LOW	

(4) Input Pins

The following table lists all input pins, indicating their active level, and whether they are synchronous or asynchronous inputs.

Name	Active Level	Synchronous/ Asynchronous	Internal Pull-up/Pull-Down
CLK,CLK2			
RESET	HIGH	Asynchronous	
SRESET	HIGH	Asynchronous	Pull-down
HOLD	HIGH	Synchronous	
AHOLD	HIGH	Synchronous	Pull-up
EADS	LOW	Synchronous	Pull-up
BOFF	LOW	Synchronous	Pull-up
FLUSH	LOW	Asynchronous	Pull-up
A20M	LOW	Asynchronous	Pull-up
BS16, BS8	LOW	Synchronous	Pull-up
KEN	LOW	Synchronous	Pull-up
RDY	LOW	Synchronous	
BRDY	LOW	Synchronous	Pull-up
INTR	HIGH	Asynchronous	
NMI	HIGH	Asynchronous	
IGNNE	LOW	Asynchronous	Pull-up
SMI	LOW	Asynchronous	Pull-up
STPCLK	LOW	Asynchronous	Pull-up
UP	LOW		Pull-up
TCK	HIGH		Pull-up
TDI	HIGH		Pull-up
TMS	HIGH		Pull-up

(5) Input/Output Pins

The following table lists all input/output pins, indicating their active level and when they are floated.

Name	Active Level	When Floated
D31-DO	N/A	Bus Hold
DP3-DPO	HIGH	Bus Hold
A31-A4	N/A	Bus, Address Hold

3. AV 9155-02 Clock Generator

3-1. General Description

The AV9155 is a low cost frequency generator designed specifically for desktop PC applications. Its CPU clocks provide all necessary CPU frequencies for 286, 386 and 486 systems, including support for the latest speeds of processors. The device uses a 14.318 MHz crystal to generate the CPU and all peripheral clocks for integrated desktop motherboards.
The dual 14.318 MHz clock outputs allows one output for the system, and one to be the input to an Avasem Graphics Frequency Generator such as the AV9116.
The CPU clock offers the unique feature of smooth, glitch-free transitions from one frequency to the next, making this theideal device to use whenever slowing the CPU speed. The AV9155 makes a gradual transition between frequencies, so that it obeys the Intel cycle to cycle timing specification for 486 systems.
The simultaneous 2X and 1X CPU clocks offer controlled skew to within 1.5ns (max) of each other.

(1) Block Diagram

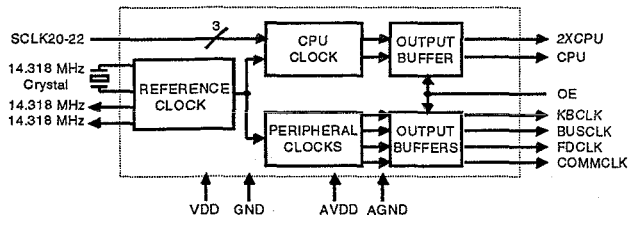


Fig. 4-2: Block Diagram

(2) Clock Table (in HH2)

a.

Clock	AV9155-02
KBCLK	12
BUSCLK	32
FDCLK	24
COMMCLK	1.84
14.318(2)	14.318

b. CPU and 2X CPU

SCLK 22 (Pin 11)	SCLK 21 (Pin 19)	SCLK 20 (Pin 20)	2XCPU (Pin 17)	CPU (Pin 18)
0	0	0	8	4
0	0	1	16	8
0	1	0	32	16
0	1	1	40	20
1	0	0	50	25
1	0	1	66.66	33.33
1	1	0	80	40
1	1	1	100	50

Note:
Refer to "Jumper and Switch Setting" section for detailed switch setting.

(3) Pin Diagram

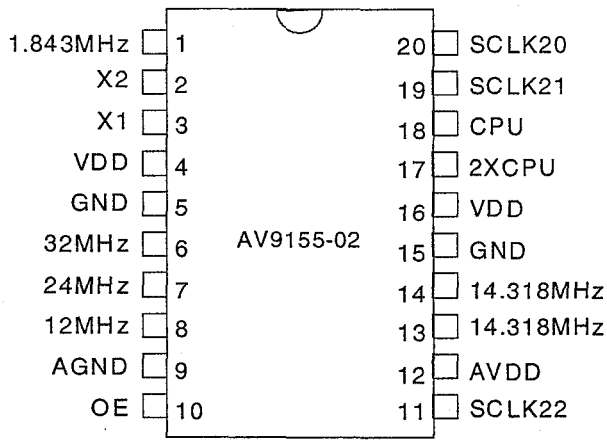


Fig. 4-3: AV9155-02 20-Pin SOIC

(4) Pin Description

Pin Name	Pin#	Pin type	Description
1.843 MHz	1	Output	1.84 MHz clock output
X2	2	Output	CRYSTAL connection. Leave as NC for clock input
X1/ICLK	3	Input	CRYSTAL connection/INPUT CLOCK
VDD	4	-	DIGITAL POWER SUPPLY (+5V)
GND	5	-	Digital GROUND
16 MHz/32 MHz	6	Output	16 MHz (AV9155-01) or 32 MHz(AV9155-02) clock output
24 MHz	7	Output	24 MHz floppy disk/combination I/O clock output
12 MHz	8	Output	12 MHz keyboard clock output
AGND	9	-	ANALOG GROUND
OE	10	Input	OUTPUT ENABLE. Tri-states all outputs when low
SCLK22	11	Input	CPU CLOCK frequency SELECT #2
AVDD	12	-	ANALOG POWER SUPPLY (+5V)
14.318 MHz	13	Output	14.318 MHz reference clock output
14.318 MHz	14	Output	14.318 MHz reference clock output
GND	15	-	Digital GROUND
VDD	16	-	DIGITAL POWER SUPPLY (+5V)
2X CPU	17	Output	2X CPU clock output
CPU	18	Output	1X CPU clock output
SCLK 21	19	Input	CPU CLOCK frequency SELECT #1
SCLK 20	20	Input	CPU CLOCK frequency SELECT #0

3-2. ELECTRICAL CHARACTERISTICS

Actual Output Frequwncies using a 14.318 MHz input. All frequencies in MHz.

SCLK22 (Pin 11)	SCLK21 (Pin 19)	SCLK20 (Pin 20)	2XCPU (Pin17)	CPU (Pin 18)
0	0	0	750	3.75
0	0	1	15.51	7.76
0	1	0	32.22	16.11
0	1	1	40.09	20.05
1	0	0	50.11	25.06
1	0	1	66.82	33.14
1	1	0	80.18	40.09
1	1	1	100.23	50.11

PERIPHRAL CLOCKS

COMMCLK (Pin 1)	BUSCLK (Pin 6)	FDCLK (Pin 7)	KBCLK (Pin 8)
1.84	32.01 or 16.00	24.000	12.0

REFERENCE CLOCKS

REFCLK1 (Pin 13)	REFCLK2 (Pin 14)
14.318	14.318

4. Pico Power Pt86C268 AT Chipset

(1) Pin Diagram

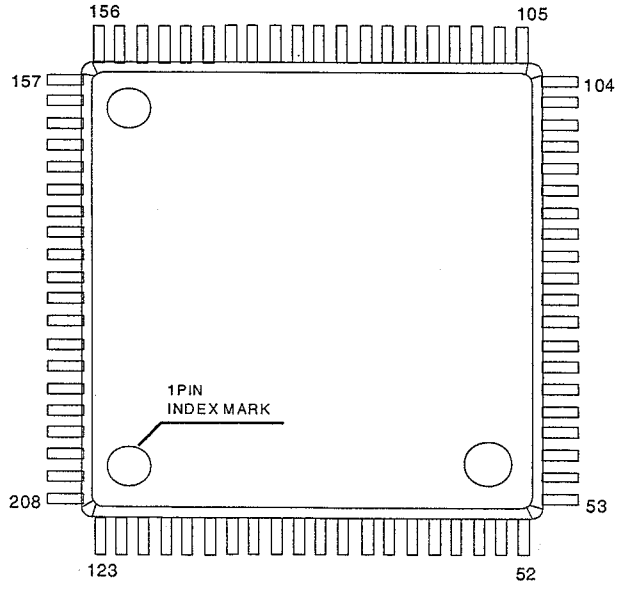


Fig. 4-4: PT86C268 Pin Diagram

(2) Pin Description

Clock and Reset Interface

Pin Name	I/O	Pin Description	Pin#
CLK2IN	I	2X Clock Input: This input clock must be two times the CPU clock speed with a 50/50 duty cycle.	42
CPUCLK	I/O 8mA	CPU Clock Output: This will be either a 1X or a 2X clock output for a 486 CPU, or a 2X clock output for the a 386 CPU as determined by an RC-RESET option select. Pleaesee section9.1.0.	109
CLKSEL (BUSTYI)	I/O 2mA	Clock Select: This output selects the 2X clock source option on the Intel 486LP CPU's. This pin is also used as BUSYI input from 387 in 386DX mode.	164
SCLK206	O 2mA	System Clock 206: This is an approximately 8MHz output to the Timer in the 82C206 Peripheral Controller.	124
TMRCLK	O 2mA	Timer Clock: This output is a 1.2MHz clock used to drive the timer in the 82C206 Peripheral Controller.	126
$\overline{\text{RCRST}}$	I	$\overline{\text{RC-RESET}}$: This input is used to reset the Evergreen HV's Power Management Controller upon initial system power-up. It should have a pull-up resistor ried to the same power source as the Evergreen HV.	162
PWRGOOD	I	Power Good Input: This input causes a complete system reset when it is drive low by the PWRGOOD signal from the power supply or a reset switch.	139
RSTDRV	O 12mA	AT Bus Reset Output: This output provides a system reset to the AT Bus and Peripherals.	97
RSTCPU	O 2mA	CPU Reset Output: This is the reset output to the CPU	185
SPNDNRST	O 2mA	Suspend Not Reset: This output provides a reset equivalent to RSTDRV except when in suspend mode. Any device not powered down during suspend mode should use this reset.	55

CPU Interface

Pin Name	I/O	Pin Description	Pin#
A<31.26:24, 16:2>	I/O 4mA	CPU Addresses. A<31.26:24.16:2>: These ars address inputs from the CPU. These pins also output DMA and Refresh addresses.	5.4-2 202-192179 -176
A<23:17	I	CPU Addresses. A<23:17>: These are address inputs irom the CPU .	I. 208-203
BE<3:0>	I	CPU Byte Enables <0.3>#: These inputs from the CPU control selection of individual bytes of data.	13-10
D<15:0>	I/O 4mA	CPU Data <15:0>: These are the low word of CPU data.	29-16 184.183
ADS	I	Address Status: This input from the CPU indicates the presentation of a valid address and cycle definition from the CPU.	188
(SMIACT) (SMIADS)	I I	*System Management interrupt Active Status: This input from some CPU's indicates that an SMI routine is in progress.* System Management Interrupt Address Starus#: This input indicates the presentation of a valid SMI address and cycle detinition on some CPU's.	187
W/R	I	Write/read #: This Input From the CPU Indicates Whether the Current Cycle is a Write or Read Access.	7
D/C	I	Data/Code : This Input From the CPU Indicates Whether the Current Cycle is a Data or Code access.	9
M/IO	I	Memory/IO: This Input From the CPU Indicates Whether the Current Cycle is a Memory or I/O access.	8
(EADS) (ERRORO)	O 2mA	External Address Valid: This Output to the 486 CPU indicates thst a valid address has been drive onto the CPU address bus which the 486 will use for an internal cache invalidation cycle.	34
RDY	/O 4mA	Read: This output to the CPU indicates completion of the current bus cycle. This pin is also an input to monitor completion of local bus cycles.	15
(BRDY) (PEREQO)	/O I4mA	Burst Ready : This output to the 486 CPU indicates completion of the current access and indicates that the CPU may burst the subsequent access. This pin is also an input to monitor completion of local bus cycles.	14
(BLAST) (PEREQI)	I	Bures Last : This input from the 486 CPU Indicates thst next BRDY# will complete the current burst cycle.	186
(FERR) (ERRORI)	I	Floating Point Error : This input from the 486DX CPU indiccates a 486DX internal floating point error.	33
(IGNNE) (BUSYO)	O 2mA	Ignore Numeric Error : This output to the 486DX CPU indicates thst floation point errors should be ignored.	36
KEN) (RSTNPU)	O 2mA	Cache Enable : This outputto the 486 CPU indicates that the current bus cycle in cacheable.	30
NMI	O 2mA	Non Maskable Interrupt: This output to the CPU indicates the occurrence of a Non Maskable Interrupt.	35
A20M	O 2mA	Address Bit 20 Mask : This output to the 486 CPU indicates thst the CPU should nask A20 in order to emulate the 8086 address wrap around.	32
HOLD	O 2mA	Hold Request: This output to the CPU indicates a request to hold the Request.	6
SRESET) (SMIRDY) (GPOB0)	O 4mA	*Soft reset : This output to some CPU's indicates a software generated CPU reset request.* System Management Interrupt Ready #: For some CPU's this output indicates completion of an SMI bus cycle. General Purpose Output B0: if not used for either of the orther optionnal functions this pin may be used as a GPO. Please see configuration register 18 for specific details.	181
(STPCLK) (IIBEN) (GPOBI)	O 4mA	*Soft reset : For some CPU's this output to the CPU toindicates a stop clock request.* I/O Instruction Break Enable #: This output drives the IIBEN# input of some CPU's. General Purpose Output BI: if not used for either of the orther optional functions this pin may be used as a GPO. Please see configuration register 18 for spacific details.	182
LOCAL	i	Local Device : This input from a local bus device indicates that tha local device has claimed the current CPU cycle and it should therefore be ignored by the Evvergreen HV.	37

DRAM Interface

Pin Name	I/O	Pin Description	Pin#
DRAMW	O 12mA	DRAM Write Enable : This output drives Write Enable for all DRAM's.	175
RAS<3.0>	O 12mA	Row Address Strrobes <3.0>: These output drive the RAS# inputs on DRAM banks 3 to 0.	4777
CAS<3:0>	O 12mA	Column Address Strobes <3.0> : These output drive the RAS# inputs on DRAM bytes 3 to 0.	169, 168, 166.52
MA<10:0>	I/O 12mA	Memory Address <10:0> These output drive the MA Lines for all DRAM's They are also used as RC-RESET configuration inputs during power up. Please see section 10.0.1.	174-171, 5148, 40-38

Peripheral Controller Interface

Pin Name	I/O	Pin description	Pin#
ASRTC	O 2mA	Address Strobe for Real Time Clock: This output Drives the Address Styobe of the 82C206's internal Real Time Clock.	130
HRQ	I	Hold Request: This input from the 82X206 indicates a request to hold the CPU and float its bus.	132
HLDA206	O 2mA	Hold Acknowledge 206: This output drives the HLDA input of the 82C206.	133
INTR	I	Interrupt Request: This input from the 82C206 indicates an interrupt reqest to the CPU.	129
INTA	O 2mA	Interrupt Acknowledge : This output to the 82C206 indicates an Interrupt Acknowlege from the CPU.	116
GATE2	O 2mA	GATE 2: This output drives the GATE2 input of the 82C206's internal Timer 2.	119
OUT2	I	OUT 2: This input is driven from the 82C206's internal Timer 2 Output.	117
ADSTB8	I	Address Strobe 8 bit; This input from the 82C206 indicates an 8 bit DMA Address.	128
ADSTB16	I	Address Strobe 16 bit: This input from the 82C206 indicates an 16 bit DMA Address.	127
IRQ13	O 2mA	Interrupt Request 13: This input from the 82C206 Peripheral Controller indicates a numeric coprocessor interrupt request.	123
REFREQ	I	Refresh Requset: This input from the 82C206 Peripheral Controller indicates a refresh request.	118
AEN8	I	Address Enable 8 bit : This input indicates an 8 bit DMA Cycle.	120
AEN16	I	Address Enable 16 bit: This input indicates an 16 bit DMA Cycle.	121
AEN206	O 2mA	Address Enable 82C206 : This output drives the 82C206's ACK input.	134

AT Bus Interface

Pin Name	I/O	Pin Description	Pin#
SA<7.0>	O 12mA	Slot Addresses<7:2>: These outputs are buffered from the equivalent CPU addresses to drive the SA Bus.	69-71, 73. 92, 93
SA<1:0>	O 12mA	Slot Addresses <1.0>: These outputs are decoded from the CPU byte enables to drive these AT Bus address lines.	95, 96
SD<15.0>	O 12mA	Slot Data<15:0>:These I/O are the data read and write path for the AT Bus.	110, 111. 113, 114. 75-77. 79, 64-67. 87-90
BALE	O 12mA	Buffered Address Latch Enable: This output is driven to the AT Bus where it indicates the presence of a valid address on the Bus.	109
$\overline{\text{MASTER}}$	I	$\overline{\text{Master}}$: This input from the AT Bus indicates thst a slot master has take control of the AT Bus.	105
$\overline{\text{MEMR}}$	O 8mA	$\overline{\text{Memory Read}}$: This output to the AT Bus indicates a Memory Read cycle to any valid AT Bua address. This pin aslo acts as an input to provide for MASTER access to local DRAM.	100
$\overline{\text{MEMW}}$	O 8mA	$\overline{\text{Memory Write}}$: This output to the AT Bus indicates a Memory Write cycle to any valid AT Bua address. This pin aslo acts as an input to provide for MASTER access to local DRAM.	102
$\overline{\text{SMEMR}}$	O 12mA	$\overline{\text{Slot Memory Read}}$: This output to the AT Bus indicates a Memory Read cycle within the 0 to IMB address range.	86
$\overline{\text{SMEMW}}$	O 12mA	$\overline{\text{Slot Memory Write}}$: This output to the AT Bus indicates a Memory Write cycle within the 0 to IMB address range.	85
$\overline{\text{IOR}}$	O 12mA	$\overline{\text{I/O Read}}$: This output to the AT Bus indicates an I/O Read cycle.	99
$\overline{\text{IOW}}$	O 12mA	$\overline{\text{I/O Write}}$: This output to the AT Bus indicates an I/O Write cycle.	98
$\overline{\text{MEMCS16}}$	I	Memory Chip Select 16 Bit #: This input from the AT Bus indicates that the current access is to a 16 bit memory device.	103
$\overline{\text{IOC16}}$	O 8mA	$\overline{\text{I/O Chip Select 16 bit}}$: This impuy from the AT Bus indicates that the current access is to a 16 bit I/O device.	108
$\overline{\text{SBHE}}$	O 12mA	$\overline{\text{Slot Byte High Enable}}$: This output to the AT Bus indicates a data transter on the high byte of the Slot Data Bus.	115
$\overline{\text{IOCHCK}}$	I	$\overline{\text{I/O Channel Check}}$: This input indicates a parity error from some device on the AT Bus.	81
IOCHRDY	I	I/O Channel Read: When this input is driven low it indicates thst the deviceon AT Bus currently being accessed requirs additional time to complete the cucle.	80
$\overline{\text{ZWS}}$	I	$\overline{\text{Zero Wait State}}$: This input from the AT Bus indicates that the device currently bring accessed can complete the cycle with zero wait stares.	74
TURBOBUS	O 12mA	TurboBus: This output is driven high on TurboBus cycles in order to shield the AT Bus from substandard commend strobes.	131
SYSCLK	O 12mA	System Clock: This output to the AT Bus provides an approximate 8MHz clock.	82
AEN	O 12mA	Address Enable: This output to the AT Bua indicates that the DMA conntroller has taken control of the CPU address bus and the AT Bus command lines.	104
$\overline{\text{REFRESH}}$	O 12mA	$\overline{\text{Refresh}}$: This output drives the AT Bus to indicates a Memory Reiresh Cycle.	107

Buffer control

Pin Name	I/O	Pin Description	Pin#
SDDIR	O 2mA	Slot Data Driection: This output drices the DIR control of the D<31:16>to SD<15:0> transceiver.	157
$\overline{\text{SDEN2}}$	O 2mA	$\overline{\text{Slot Data Enable 2}}$: This output drices the G# of the D<23:16>to SD<7:0> transceiver.	158
$\overline{\text{SDEN3}}$	O 2mA	$\overline{\text{Slot Data Enable 3}}$: This output drices the G# of the D<31:24>to SD<15:8> transceiver.	159
XDDIR	O 2mA	Extended Data Direction: This output drives the DIR controlof the optional XD to SD transceiver.	138
MDDIR (GPIOAI) (ELB1)	I/O 2mA	Buffer Direction : This output drives the DIR input of the optional D to MD transceiver. This pin may also be used as an optional GPIO. Please see configuration register 18 for specific details.	165
$\overline{\text{MDEN}}$ (GPIOAI) (ELB1)	I/O 4mA	Buffer Enable : This output drives the G# input of the optional D to MD transceivers. This pin may also be used as an optional GPIO. or an Extended Low Battery Detecl. Please see configuration register 18H for specific details.	160

Power Management Interface

Pin Name	I/O	Pin Description	Pin#
32KIN	I	32KHL Input: This input is used to count the refresh interval during Suspend Mode.	153
14MHZIH	I	14.318 Mega Hertz Input: This input is used to generate the timer clock for the 82C206 Peripheral Controller.	122
(KBCLKI) (GPIOC0)	I/O 4mA	Keyboard Clock Input: This input generate the Keyboard Clock Output. This pin may also be used as an optional GPIO. Please see register section 10.4.18 for specific details.	57
(KBCLKO) (GPIOC0)	I/O 4mA	Keyboard Clock Output: This output drives the Keyboard Controller clock input. This pin may also be used as an optional GPIO. Please see register section 10.4.18 for specific details.	58
(PMI) (IRQX) (SMI)	I/O 4mA	Power Management Interrupt: This output indicates a power manegement interrupt. It should be connrcted to either IRQX for a Non-SMI CPU or to SMI for any SMI compatible CPU.	180
PC<4:0>	O 2mA	Power Control<4:0>:These output provides inividual power control for five system components.	146-142

(Continued)

Pin Name	I/O	Pin Description	Pin#
(PC<5>) (LEDFLSH)	O 2mA	Power Control<5>: This Output provides individual power contril for one system component. LED Flacher: This output can optionally be used to control one or more flashing LED's to indicate verious system status conditions such as Low Battery or Suspend Mode. Please see register section 6.5 for more details.	147
PC<6>	O 2mA	Power Control<6>: This Output provides individual power contril for one system component.	148
PC<7>	O 2mA	Power Control<7>: This Output provides individual power contril for one system component.	149
PC<8>	O 2mA	Power Control<8>: This Output provides individual power contril for one system component.	150
(PC9) (PCBKLT)	O 2mA	Power Control<8>: This Output provides an individual power contril for one system component. Power Control for Backlight: This ouyput can optionally be controlied directly by the peripheral/backlight timer. Please see sections 5.5.5 and 10.4.13 for more details.	151
DPIO <3.0>	I/O 4mA	General purpose I/O's <3:0>: These four I/O's are provided for general purpose usage.	54.53 156. 155
RING	I	Ring: This input provides for a "wake-up" call from a modem.	152
SWTCH	I	Switch: This input provides an on-off function between Fully-On and Standby Modes.	140
EXTACT	I	External Activity: This input indicates thst there is current external activity.	161

Battery Manegement Interface

Pin Name	I/O	Pin Description	Pin#
ACPWR	I	AC Power: This input indicates that the current power source is AC.	135
LB	I	Low Battery: This input from the power supply indicates a low battery condition.	136
VLB	I	Very Low Battery: This input from the power supply indicates a very low battery condition.	137

System Miscellaneous

Pin Name	I/O	Pin Description	Pin#
$\overline{\text{KBDCCS}}$	I/O	Keyboard Controller Chip Select #: This ouypuy drives the 8042, or equivalent, Keyboard Controller Chip Select.	59
$\overline{\text{ROMCS}}$	O 2mA	ROM Chip Select #: This output drives the BIOS ROM Chip Select.	60
SPKR	O 2mA	Speaker: This output drives the system apeaker.	63
VDDCL <1:0>	--	Core Logic Power Pins	61, 141
VSSCL <0:1>	--	Core Logic Power Pins	163, 83
VDDIO <9:0>	--	I/O Power Pins	43, 167. 191. 62. 68. 78. 91. 101. 112. 154
NSSIO <8:0>	--	I/O Ground Pins	41. 56. 72. 84. 94. 106. 125. 170. 189.

Muliti-Function NPU Pins

The interface control signals between a 386DX and a 387 NPU are significantly different from those used in a 486 system. In order to save pins these seversl signals unique to 386 implementation are shared with several signals uniqur to the 486. The following table indicates which pins are shared and described the 386 function of each.

Multi-function Pins -- 486 vs 386DX

486 NAME	386 NAME	I/O	386 DESCRIPTION	PAD I/O
$\overline{\text{EADS}}$	$\overline{\text{ERRORO}}$	O	Error output: This pin is the moditied ERROR output to the 386DX.	O
$\overline{\text{BLAST}}$	PEREQI	I	Processor Extension Request Input: This input from a 387 indicates an NPU cycle request.	I
$\overline{\text{BRDY}}$	PEREQO	O	Processor Extension Request Output: This output from a 387 indicates an NPU cycle request.	O
$\overline{\text{FERR}}$	$\overline{\text{ERRORI}}$	I	Error Input: Thispin is the ERROR input from a 387 NPU.	I
$\overline{\text{IGNNE}}$	$\overline{\text{BUSYO}}$	O	Busy Output: This output to a 386DX indicates that the NPU is executing NPU cycles.	O
$\overline{\text{KEN}}$	RSTNPU	O	Reset NPU: This output signals a reset for a 387 NPU.	O
CLKSEL	$\overline{\text{BUSYI}}$	I	Busy Input: This input from the a 387 NPU indicates that it is executing NPU cycleS.	I/O

5. Memory Controller

5-1. Description

The PT86C268 implements a high performance Burst Mode DRAM Controller for optimal 486 system performance.
In addition to the Burst Mode capability, the PT86C268 also incorporates Page Mode operation. This takes advantage of the DRAM's built in Page Mode feature to allow faster memory accesses within a selected row--also known as a page.
The memory capacity of the PT86C268 is up to four banks and 64M bytes of local DRAM. The maximum memory size would be achieved by installing 4 banks of 4M DRAM's which provide 16M bytes per 32 bit bank for a total of 64M. In addition the four bank capability is very useful with lower density DRAM's such as the 256K and 512K which provide 1M and 2M per 32 bit bank respectively.
The PT86C268 provides unlimited flexibility by allowing virtually any combination of standard DRAM's. The basic memory types supported are, 256K x4, 256K x 16, 512K x 8, 1M x 1, 1M x 4, 4M x 1, and 4M x 4. The Evergreen HV provides unlimited flexiblity of installation by allowing the manufacturer or user to plug in any combination of different DRAM types in any order. And the entire memory configuration procedure can be handled automatically by a simple BIOS routine.

5-2. DRAM Timing Control

1. DRAM Timing Programmability

IN order to allow the system designer to best optimize for their specific system configurations, the PT86C268 DRAM Controller has included programmable options for several of the most critical DRAM timing parameters. Following are brief descriptions of the programmable options.
RAS Precharge: The RAS Precharge time for a page miss cycle can be programmed to either 0 or 1 wait state. With 0 wait states the RAS precharge time will be 2.5 CLK2's. And with I wait state the RAS precharge time will be 4.5 CLK2's.
RAS Precharge Stretch: For some conditions the RAS Precharge may not need a full wait state. In these cases the RAS Precharge can be programmed for a half clock stretch which will improve pertormance and save power. With the half clock stretch the RAS precharge time will be 3.5 CLK2's.
CAS Precharge: The Read-CAS Precharge time should be set to 0.5 CLK2's when the Read-CAS Pulse Width is programmed to 0 wait states, and it should be set to 1 CLK2 when the Read-CAS Pulse Width is programmed to I wait state.
Read-CAS Pulse Width: The Read-CAS Pulse Width can be programmed to either 0 or 1 wait states. With 0 wait states the Read-CAS Pulse Width will be 1.5 CLK2's. And with 1 wait state the Read-CAS Pulse
Width time will be 3 CLK2's.
Read-CAS Stretch: For some conditions the Read-CAS pulse width may not need a full wait state. In these cases the Read-CAS can be programmed for a half clock stretch which will improve performance and
save power. With the half clock stretch the Read-CAS Pulse Width will be 2.5 CLK2's.
Write-CAS Pulse Width: The Write-CAS Pulse Width can be programmed to either 0 or 1 wait states. With 0 wait states the Write-CAS Pulse Width will be 1 CLK2. And with 1 wait state the Write-CAS Pulse Width time will be 2 CLK2's.
Please see register sections 10.3.2-3 for specific details on the programming of DRAM timings.

2. Automatic Page Sizing

The minimum page size for each bank of DRAM is determined by the smallest type of DRAM installed, with the default being 2KB per page. With 256K or 512K memory installed the page size will always be limited to 2K. However, if the minimum memory size installed is M or 4M then the page size can be increased to 4KB or 8KB respectively. This page resizing can also be done automatically by the BIOS at the same time that it evaluates memory types and calculates starting addresses. The advantage of the larger page sizes is a slightly higher hit rate for the page mode DRAM Controller.

Minimum Page Size = 2KB											
MA	10	9	8	7	6	5	4	3	2	1	0
RAS	A22	A20	A19	A18	A17	A16	A15	A14	A13	A12	A11
CAS	A23	A21	A10	A9	A8	A7	A6	A5	A4	A3	A2

Minimum Page Size = 4KB											
MA	10	9	8	7	6	5	4	3	2	1	0
RAS	A22	A20	A19	A18	A17	A16	A15	A14	A13	A12	A11
CAS	A23	A21	A10	A9	A8	A7	A6	A5	A4	A3	A2

Minimum Page Size = 8 KB											
MA	10	9	8	7	6	5	4	3	2	1	0
RAS	A22	A20	A19	A18	A17	A16	A15	A14	A13	A12	A11
CAS	A23	A21	A10	A9	A8	A7	A6	A5	A4	A3	A2

5-3. Refresh Controll

1. Hidden AT Bus Refresh

The PT86C268 implements a hidden AT Bus refresh mechanism. This hidden refresh works by decoupling the AT Bus from the CPU Bus and from local memory, such that AT Bus refresh cycles may occur simultaneously with CPU accesses to local memory. The result is that AT Bus refresh cycles no longer hold up the CPU since they occur in parallel with normal CPU operation. This parallelism provides a significant increase in system performance, typically on the order of 5%. The 5% savings is directly attributable to the amount of time normally used up by the AT Bus refresh cycle due to its slow
clock and the associated hold synchronization time. And although the AT Bus refresh is hidden, its operation on the bus is still completely AT compatible, including the standard AT refresh counter and RAS-only refresh control logic.

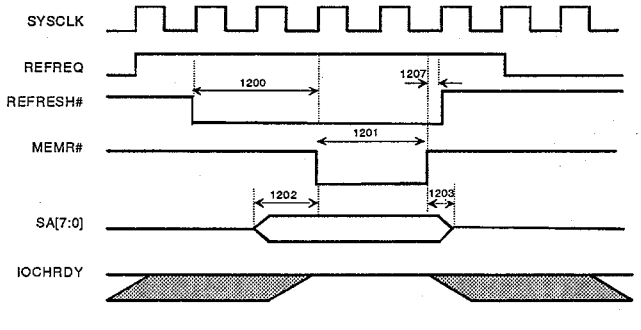


Fig. 4-5: AT Bus Refresh Timing

2. Staggered CAS Before RAS Refresh of Local DRAM

CAS before RAS refresh is provided for local DRAM under periodic control of either system timer two or the dedicated Evergreen HV refresh timer. CAS before RAS is a very efficient refresh method in
that it utilizes refresh address counters internal to the DRAM. This means that a refresh address need not be driven from the Evergreen HV, only the CAS and RAS lines are asserted. In addition the RAS
lines are staggered in time to minimize the associated power surge. Further, since the local memory refresh is completely decoupled from the AT Bus refresh, the local memory can always use the slow
refresh option.

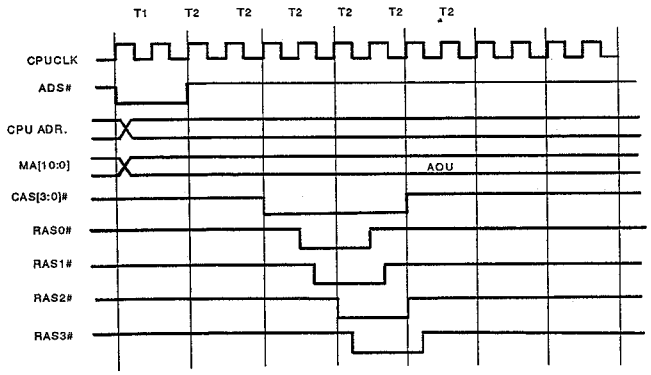


Fig. 4-6: Local DRAM Refresh in CPU Mode

5-4. Shadow RAM Control

The shadow RAW feature provides significant preformance enhancement on BIOS accesses. This feature is used by first copying the contents of any shadowable ROM from the ROM itself to DRAM located at the same address space. The transfer is made by first enabling the appropriate address space to the ROM Read/DRAM Write Mode. When enabled this mode provides that each memory read access is directed to the ROM and each memory write access is directed to the DRAM, such that each address can be read and immediately written back to perform the transfer. Once the transfer is complete the ROM has been "shadowed" in DRAM and the appropriate region of address space should then be set to the DRAM Read Only Mode. The entire BIOS region from C0000 to FFFFF is shadowable in the following increments.

Address Range	Segments	Block Size
F0000 to FFFFF	1	64K
C0000 to EFFFF	12	16K

5-5. ROM

1. Single 8 Bit BIOS ROM

The PT86C268 provides for a single 8 bit BIOS ROM in order to save both space and power. All necessary cycle conversion from 16 to 8 bit cycles is handled internally by the AT Bus Controller to provide the simplest possible BIOS ROM interface. This cycle conversion process takes longer to access the ROM since it converts one 16 bit cycle into two 8 bit cycles but this should not impact system performance since the BIOS ROM will typically be shadowed during system initialization.

2. Combined System & Video BIOS ROM

In order to provide the optimum in space and power savings, the PT86C268 provides the option of combining the system and video BIOS's into a single ROM. This option combined with the single 8 Bit BIOS ROM reduces the total ROM count from three for a typical AT system to only one for an Evergreen HV Portable.

3. Flash ROM Support

The Evergreen HV provides support for Flash ROM's through conditional control of the ROM$\overline{CS}$ pin. The FLASHENB bit in register 300H enables a Flash ROM to be written by providing a valid ROM chip select for any memory write to the ROM address range. Normally ROM$\overline{CS}$ would only be active on memory reads. When FLASHENB is low ROM$\overline{CS}$ will only respond to memory reads. With this implementation, the $\overline{MEMW}$ command can be directly connected to the program pin on the Flash ROM. Writes will only be effective, however, when the ROM$\overline{CS}$ is valid which means only when the FLASHENB bit is set high.

5-6. AT Bus Controller

The AT Bus Controller handles all operations to the AT Bus. This inciudes the monitoring of $\overline{IOCS16}$ and $\overline{MEMCS16}$ to determine byte or word data size, the monitoring of IOCHRDY and $\overline{ZWS}$ to determine appropriate cycle length, and as weill it includes the management of all data direction and drive controls. In addition the AT Bus Controller handles all cycle conversion requirements. These include conversion from double-word cycles to word or byte cycles and word to byte conversion as required by word or byte devices.

1. Quiet Bus

The Evergreen HV implements a Quiet Bus whereby none of the AT Bus signals will be driven by the Evergreen HV except during cycles that are specifically directed to the AT Bus. This restriction provides two advantages. First, this prevents slow devices on the AT Bus from being confused by the substandard pulse widths created by non-AT Bus cycles that run at higher speeds. And second, this feature also helps to reduce power consumption by avoiding the conventionally wasteful routine of needlessiy charging and discharging the significant capacitive loads on the AT Bus.

2. AT Bus Clock Generation

The Evergreen HV generates the AT Bus Clock by dividing down from the CLK2IN to an approximate 8 MHZ frequency. This has the distinct advantage of keeping the AT Bus Clock synchronous to the CPU clock, which removes the need for a second oscillator and simplifies the AT clock synchronization process. The appropriate divisor for the At Bus Clock depends on the speed of the CPU. The following table indicates the divisors supported and which apply at each CPU clock frequency to achieve an approximate 8MHZ Bus speed. The appropriate divisor must be selected by a configuration register option. Please see register section 10.2.0 for specific details on programming the appropriate divisor.

CPU Clock	CLK2IN	Divide CLK2IN by
16MHZ	32MHZ	4
20MHZ	40MHZ	5
25MHZ	50MHZ	6/7
33MHZ	66MHZ	8/9

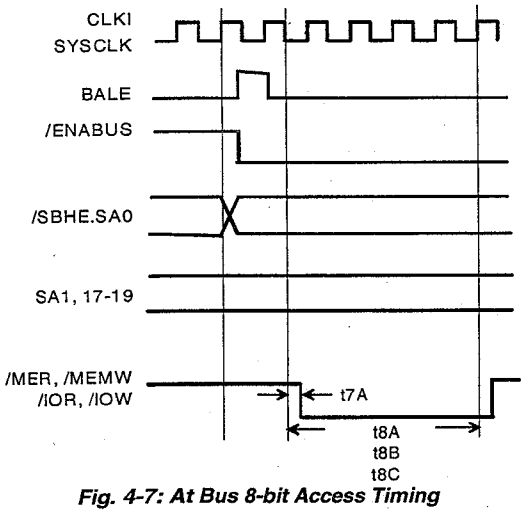
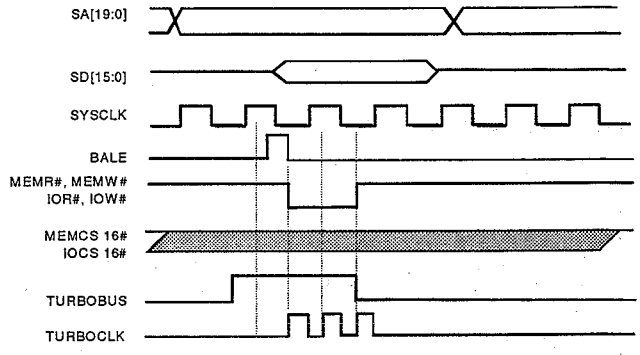


Fig. 4-7: At Bus 8-bit Access Timing

5-7. TurboBus

Many devices on the AT Bus are capable of operating at higher than the standard 8MHZ Bus speed. This generally presents a compatibility problem, with other devices on the Bus that cannot run any faster than 8MHZ. The PT86C268 provides a TurboBus option which provides a "best of both worlds" solution. This option allows selected devices to operate at higher speeds without compromising compatibility with slower devices. All devices are connected to the common AT Bus but the frequency of each AT Bus operation is determined by a programmable address decode to be either a standard frequency operation or a TurboBus operation. In addition, the PT86C268 provides a TURBOBUS control output which may be used to shield slower devices from being confused by the TurboBus cycles. Any Turbo devices should be connected directly to the PT86C268 command strobe outputs, while devices requiring the standard AT Bus speed should be connected to the output of the tri-stateable transceiver between the PT86C268 and the AT Bus. The output enable of this transceiver should be connected to the TURBOBUS control pin. The TURBOBUS signal will be driven high on any TurboBus cycle thereby disconnecting the command strobes of slower devices during high speed cycles. Aside from the reference speed of the bus cycle most bus mechanisms operate in the same manner as the standard 8MHZ AT Bus. Like the standard AT Bus speed, the TurboBus speed is also selected as a division of the CLK2IN frequency. The range of divisors supported is from 3 to 9.



TURBOCLKIS AN INTERNAL CLOCK

TurboBus I -- 16 Bit Memory Cycle or
TurboBus II -- 8 or 16 Bit, Memory or I/O Cycles

6. 82C206 Integrated Peripheral Controller

6-1. General Description

The 82C206 Integrated Peripheral Controller includes two 8237 DMA controllers, two 8259 interrupt controllers, one 8254 timer/counter, one MC146818 compatible real time clock, an additional 64 bytes CMOS RAM, one 74LS612 memory mapper, and some top level decoder/configuration logic circuits. It is a single chip integration of all main peripheral parts attached to the X bus of PC/AT architecture. While providing full compatibility with PC/AT architecture, the 82C206 also offers some enhanced features and improved speed performance. These include an additional 64 bytes of user definable CMOS RAM in real time clock and drastically reduced recovery time for the 8237, 8259 and 8254. Programmable wait state option is provided for the DMA cycles and CPU I/O cycles accessing this chip. This chip also provides programmable 8 or 4 MHz DMA clock selection. The 82C206 is implemented using advanced 1.5u CMOS design technology and is packaged in an 100 Pin QFP.

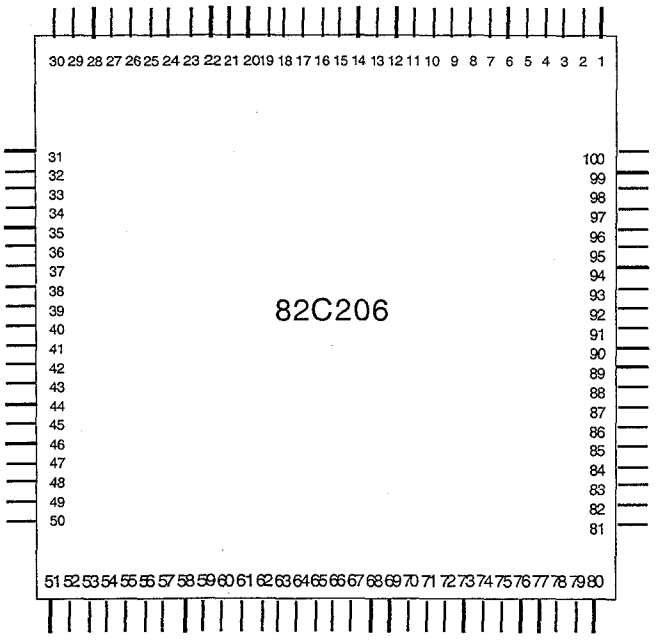


Fig. 4-8: 82C206 Pin Diagram

6-2. Pin Description

Pin#	Designation	I/O	Description
15	SYSCLK	I	CLOCK INPUT is used to generate the timing signals for DMA operation. This pin can be driven to 10 MHz frequency. The internal clock used for DMA operation is either SYSCLK or SYSCLK/2 which is a
75	OSCI	I	OSCILLATOR INPUT is used to generate the time base for the time function of real time clock. External square waves of 32.768 KHz may be connected to this pin.
10	RESET	I	RESET is an active high input which affects the following registers: DMA controller: Clears the command, status, request, temporary registers, byte pointer flip flop. Sets the mask register. Following reset, DMA controller is in the idle state. INTERRUPT controller: Clears the edge sense circuit, mask registers, all ICW4 functions. IRQ0 is assigned the highest priority. Slave address is set to 7. Special mask mode is disable and status read is set to IRR.
71	IOCHARDY	I/O	I/O CHANNNEL READY is a bidirectional pin. In the input mode, it is used to extend the memory read or write pulses for the DMA controller to access slow memories or I/O devices. It must satisfy setup and hold times with respect to the DMA internal clock in order to work reliably. A low on IOCHRDY causes the internal DMA ready signal to go low asynchronously. When IOCHRDY goes high, one DMA clock cycle will elapse before internal DMA ready signal goes high. In the output mode, it is an open drain output and provides an active low output whenever a UM82C206 internal register is accessed. It will remain low for a pre-programmed unmber of DMA internal clock cycles (as controlled by bits 7 and 6 of UM82C206 configuration register) and then goes high. In this way, IOCHRDY can insert wait states (as counted by DMA internal clock cycles) when CPU accesses the UM82C206 internal registers. This pin must be pulled up by an external resistor. In a PC/At architecture base design this pin should be wire-ORed to the PC/AT's IOCHRDY signal.

Pin#	Designation		I/O	Description
24-31	18-25	XD7-XD0	I/O	X DATA BUS are 3-state bidirectional pins which are connected to the XD bus in PC/AT architecture design. During CPU I/O write cycles, these are input pins to let CPU program the contents of UM82C206 internal registers. During DMA cycles, the most significant 8 bits of the address are output onto these pins to be strobed into an external latch by ADSTB8 or ADSTB16. During DMA memory-to-memory transfers, data from the memory comes into the DMA controller via these pins and stores in the internal temporary register during read from the memory partial cycle. In the write to memory partial cycle, the data stored in the temporary register will output via these pins again and write into the new memory location. During the interrupt acknowledge cycle, the interrupt controllers output the interrupt vector byte via these pins. These pins are also used as the multiplexed address/data bus for the real time clock and the CMOS RAM accesses.
35-43 34	31-39 41	XA8-XA0 AX9	I/O I	ADDRESS BUS are connected to the XA bus in PC/AT architecture design. XA8-XA0 pins are bidirectional pins. XA9 is an input only pin. During CPU I/O accesses to the UM82C206, XA9-XA0 are used to address configuration register and the internal registers of 8237, 8259, 8254, MC146818, CMOS RAM, 74LS612. During a CPU cycle, XA3-XA0 pins are used by the CPU to address the registers of the DMA controller corresponding to DMA channels 0-3. XA4-XA1 pins are used by the CPU to address the registers of the DMA controller corresponding to DMA channels 5-7. During a DMA cycle, XA7-XA0 pins are outputs and carry address information for DMA channels 0-3. XA8-XA1 pins are outputs and carry address information for DMA channels 5-7.
54	54	$\overline{\text{XIOR}}$	I/O	X I/O READ is a bidirectional active low 3-state pin. In a non DMA or non interrupt cycle, it is an input control signal used by the CPU to read the UM82C206 internal registers. In an active DMA cycle, it is an output control signal used by the DMA controller to access data from a peripheral druing a DMA write memory transfer.
52	50	$\overline{\text{XIOW}}$	I/O	X I/O WRITE is a bidirectional active low 3 state pin. In a non DMA or non interrupt cycle, it is an input control signal used by the CPU to write the UM82C206 internal registers. In an active DMA cycle, it is an output control signal used by the DMA controller to write data to a peripheral during a DMA read memory transfer.

Pin#	Designation		I/O	Description
61	61	$\overline{\text{DMAMER}}$	O	DMA MEMORY READ is an active low 3-state output pin used to access data from the selected memory location during DMA read memory or memory-to-memory transfer.
62	62	$\overline{\text{DMAMEMW}}$	O	DMA MEMORY WRITE is an active low 3-state outputpin used to write data to the selected memory location during DMA write memory or memory-to-memory transfer.
73	76	HLDA1	I	HOLD ACKNOWLEDGE 1 is an active high signal from the UM82C211C to indicate that the CPU has relinquished control of the system busses.
69	72	HRQ	O	HOLD REQUEST is an active high output to the UM82C211 to request control of the system bus. When a DREQ occurs and the corresponding mask bit is clear, or a software DMA request is made, the DMA controller issues HRQ to the UM82C211C. After CPU releases the system bus, the UM82C211C then issues a HLDA1 back to the UM82C206 if DMA has been permitted to control the system bus.
44-47	42-45	DREQ0-DREQ3 DREQ7	I	DMA REQUEST is an asynchronous DMA channel request input for each DMA channel. In fixed priority, DREQ0 has the highest priority and DREQ7. has the lowest priority. A Periphal device will activate a DREQ line if it needs a DMA service. DACK will acknowledge the recognition of DREQ request. DREQ must be maintained until the corresponding DACK goes active. DREQ will not be recognized while the DMA clock is stopped. Unused DREQ inputs should be kept inactive and the corresponding mask bit should be set to avoid an undesired DMA function. Polarity of DREQ is programmable. Reset initializes these lines to active high. DREQ0-DREQ3 support 8-bit transfers between 8-bit I/O device and 8 or 16-bit transfers between 16-bit I/O device and 16-bit system memory. DERQ4 is not externally available and is used to cascade DREQ0-DREQ3.

Pin#	Designation		I/O	Description
67	70	TC	O	TERMINAL COUNT is an active high signal. It indicates the completion of DMA services. A pulse is generated by the DMA controller when terminal count for any channel is reached except for channel 0 in memory-to-memory transfer mode. Druing memory-to-memory transfer terminal count will be generated when the terminal count for channel 1 occurs. When a TC pulse occurs, the DMA controller will terminate the service, and if auto-initialize is enabled, the base registers will be written to the current registers of that channel. The mask bit and TC bit in the status register will be set for the currently active channel unless the channel is programmed for auto-initialization. In that case, the mask bit remains clear.
48-51 57-55	46-49 57-55	DACK0- DACK3- DACK5- DACK7	O	DMA ACKNOWLEDGE is used to notify the individual peripherals when one has been granted a DMA cycle. Because these signals are used internally for cascading the DMA channels and for DMA page register selection, they must be programmed to active low and cannot be changed. Reset initializes them to active low.
66	69	ADSTB8	O	ADDRESS STROBE 8 is an active high output. It is used to latch the upper address byte XA8-XA15 for 8-bit peripheral devices. During DMA block transfers, ADSTB8 will only be issued when the upper address byte must be updated, thus speeding transfer through elimination of S1 states of DMA cycles. ADSTB8 is active for DMA channels 0-3.
65	65	ADSTB16	O	ADDRESS STROBE 16 is an active high output. It is used to latch the upper address byte XA9-XA16 for 16-bit peripheral devices. During DMA block transfers, ADSTB16 will only be issued when the upper address byte must be updated, thus speeding transfer through elimination of S1 states of DMA cycles. ADSTB16 is active for DMA channels 5-7.
63	63	AEN8	O	ADDRESS ENABLE 8 is an active low output. It is used to enable the latch of the upper address byte XA8-XA15 for 8-bit peripheral devices. It is inactive when external bus master controls the system
64	64	AEN16	O	ADDRESS ENABLE 16 is an active low output. It is used to enable the latch of the upper address byte XA9-XA16 for 16-bit peripheral dev ices. It is inactive when external bus master controls the system

Pin#	Designation		I/O	Description
33	30	ACK (MSE)	I	MODULE SELECT ENABLE is a two purpose input. When high, it enables the chip select function on one of the modules of UM82C206 for the CPU programming functions. When low, the UM82C206 is essentially disconnected from the system bus and is capable of performing an active DMA or an interrupt cycle. In a PC/AT architecture design, it is tied to ACK signal of main board.
5-10 11 13	95-100 1 5	A23-A16 A17 XA16	O	A23-A17 and XA16 are 3-state output pins. A23-A17 are the upper 7 bits of the DMA page register. XA16 is the least significant bit of the DMA page register and is used for DMA transfers for 8-bit peripheral devices only. XA16 is not used for 16-bit DMA transfers as XA16-XA9 being provided by demultiplexing the data bus.
76-82 83 84 1-3 4	79-85 86 87 91-93 94	IRQ15-IR Q9 IRQ7 IRQ6 IRQ5-IRQ 3 IRQ1	I	INTERRUPT RREQUESTS are asynchronous inputs. When 8259 is operating in edge triggered mode, an interrupt request is executed by raising an IRQ input low to high and holding it high until it is acknowledged by CPU. When 8259 is operating in level triggered mode, an interrupt request is executed by raising an IRQ input high and holding it high until it is acknowledged by CPU.
16	8	$\overline{\text{INTA}}$	I	INTERRUPT ACKNOWLEDGE is an active low input. It is used to enable the interrupt controllers to output the vector data on to the data bus by an interrupt acknowledge sequence from the CPU.
70	73	INTR	O	INTERRUPT REQUEST is an active high output pin. It is connected to the CPU's interrupt pin and is used to interrupt the CPU when an interrupt request occurs.
23	17	TMRCLK	I	TIMER CLOCK is an input clock for 8254 counter 0, counter 1 and counter 2. In PC/AT architecture design, it is approximately 1.19 MHz.
22	16	GATE2	I	GATE 2 is a gate input for 8254 counter 2. In PC/AT architecture design, the counter 2 is used for tone generation for speaker. It is driven by bit 0 of I/O port 61 h.
20	14	OUT1	O	OUT 1 is an output of 8254 counter 1. In PC/AT architecture design, the counter 1 is programmed as a rate generator to produce a 15 usec period signal for DRAM refresh.
19	13	OUT2	O	OUT 2 is an output of 8254 counter 2. In PC/AT architecture design, counter 2 is used for tone generation for speaker.
71	74	AS	I	ADDRESS STROBE is an active high input. It is pulsed by UM82C211C when CPU accesses the real time clock or CMOS RAM of the UM82C206. The falling edge of this pulse latches the address from the XD bus.

Pin#	Designation		I/O	Description
15	7	PSRSTB	I	POWER SUPPLY STROBE is an active low input. It is used to establish the condition of the control registers of real time clock when power is applied to the device. In PC/AT architecture design, it should be tied to the battery back-up circuit. When PSRSTB and TEST are both low, the following occurs: (a) Periodic Interrupt Enable (PIE) bit is cleared to zero. (a) Periodic Interrupt Enable (PIE) bit is cleared to zero. (b) Alarm Interrupt Enable (AIE) bit is cleared to zero. (c) Update ended Interrupt Enable (UIE) bit is cleared to zero. (d) Update ended Interrupt Flag (UF) bit is cleared to zero. (e) Interrupt Request status Flag (IRQF) is cleared to zero. (f) Periodic Interrupt Flag (PF) bit is cleared to zero. (g) The part is not accessible. (h) Alarm interrupt Flag (AF) bit is cleared to zero. (i) Square Wave output enable bit is cleared to zero.
14	6	PWRG		POWER GOOD is an active high input and is connected to the power good of the power supply in PC/AT architecture design. It must be high for bus cycles in which the CPU accesses the real time clock. When it is low, all address, data, data strobe and R/W pins are disconnected from the processor.
17	9	TEST	I	TEST is an active high input to enable the chip testing for production. It should be tied low for normal operation.
32,75	26,78	VCC		POWER SUPPLY
12,53 7 4	3,77 52	VSS		GROUND

6-3. Interrupt Controller

Description

There are two programmable interrupt controllers for the 82C206. They are fully compatible with Intel's 8259 controller, providing up to 15 interrupts sources (14 external and 1 internal). The internal line connects to the 8254 Counter 0 output. These interrupt controllers prioritize interrupt requests to the CPU.

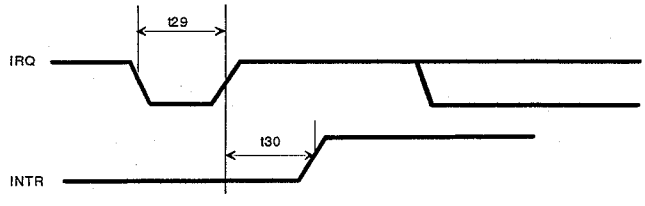


Fig. 4-9: Interrupt Timing

(1) Interrupt Controller Channel Assignment

IRQ 0 - Timer Channel 0
IRQ 1 - Keyboard (Output Buffer Full)
IRQ 2 - Interrupt from Controller 2
IRQ 3 - Serial Port (Secondary)
IRQ 4 - Serial Port (Primary)
IRQ 5 - Parallel Port 2
IRQ 6 - FDD Controller
IRQ 7 - Parallel Port 1
IRQ 8 - Real Time Clock Interrupt
IRQ 9 - Software Redirected to INTOAH (IRQ2)
IRQ 10 - Reserved
IRQ 11 - Reserved
IRQ 12 - Reserved
IRQ 13 - Co-processor
IRQ 14 - HDD Controller
IRQ 15 - Reserved

6-4. DMA

Description

The 82C206 has two DMA controllers, compatible with the Intel 8237, which provide a total of seven DMA channels. Combined with the Memory Mapper, each DMA channel has a 24-bit address output to access data throughout the 16MB system address space. Channel 0 through channel 3 support 8-bit peripherals,
transferring data to or from an 8-bit memory. Each channel can transfer data in 64kB pages. Channel 4 is used for cascading and is not available externally. Channel 5 through channel 7 support 16-bit
I/O adapters, transferring data a word at a time. These channels can transfer in 128kB pages.

DMA Channel No.	Function
0	Spare
1	SLDC
2	Diskette
3	Spare
4	Spare
5	Spare
6	Spare
7	Spare

*Synchronous Data Link Control Communication

6-5. Memory Mapper

The 82C206 has a built-in equivalent logic to the 74LS612, generating the upper address bits during a DMA cycle.

Source Memory Mapper 8237
(for DMA Channels 0-3)
Address A23 <---------- >A16 A15 <---------- >A0
(For DMA Channels 5-7)
Address A23 <---------- >A17 A16 <---------- >A1

6-6. Timer/Counter

The 82C206 provides three internal counters which are compatible with the 8254. The clock input for each counter is tied to a clock of 1.19MHz, which is derived by dividing the 14.318MHz crystal input by 12. The output of Counter 0 is connected to the IRQ0 input of interrupt controller 1. Counter 1 initiates a refresh cycle and Counter 2 generates sound waveforms for the speaker.

6-7. I/O Address Map

Hexadecimal Range	Devices	Usag
000-01F	DMA controller 1	System
020-03F	Interrupt controller 1	System
040-05F	Timer	System
060-06F	Keyboard I/O	System
070-07F	Real time clock, NMI mask	System
080-09F	DMA page register	System
0A0-0BF	Interrupt controller 2	System
0C0-0DF	DMA controller 2	System
0F0	Clear math coprocessor busy	System
0F1	Reset math coprocessor	System
0F8-0FF	Math coprocessor	System
1F0-1F8	Fixed disk	I/O
200-207	Game	I/O
278-27F	Parallel printer port 2	I/O
2F8-2FF	Serial port 2	I/O
300-31F	Prototype card	I/O
360-36F	Reserved	I/O
378-37F	Parallel printer port 1	I/O
380-38F	SDLC, Bi-synchronous 2	I/O
3A0-3AF	Bi-synchronous 1	I/O
3B0-3BF	Mono display printer adapter	I/O
3C0-3CF	Reserved	I/O
3D0-3DF	Color/graphic monitor adapter	I/O
3F0-3F7	Floppy diskette controller	I/O
3F8-3FF	Serial port 1	I/O

7 (Keyboard Controller)

7-1.

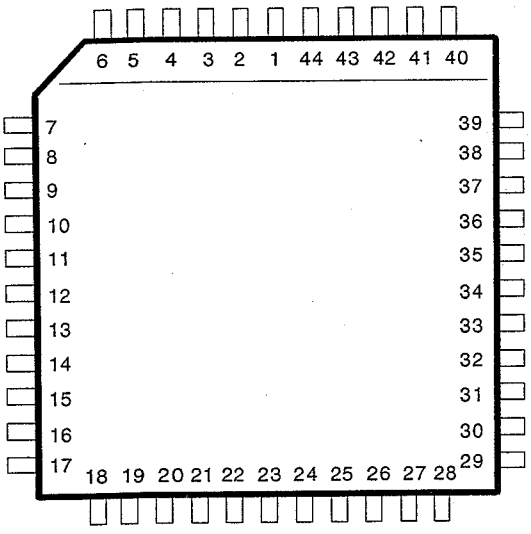


Fig. 4-10: UPI-C42 Keyboard Controller

(1) Pin Description

Symbol	Pin	Type	Description
TEST 0, TEST 1	2 43	I	TEST INPUTS: Input pins which can be directly tested using conditional branch instructions. FREQUENCY REFERENCE: TEST 1 also functions as the event timer input (under software control). TEST 0 is used during PROM programming and ROM/EPROM verification. It is also used during Sync Mode to reset the instruction state to S1 and synchronize the internal clock to PH1.
XTAL1, XTAL2	3 4	I I	INPUTS: Inputs for a crystal, LC or an external timing signal to determine the internal oscillator frequency.
$\overline{\text{RESET}}$	5	I	RESET: Input used to reset status flip-flops and to set the program counter to zero. $\overline{\text{RESET}}$ is also used during EPROM programming and verification.
$\overline{\text{SS}}$	6	I	SINGLE STEP: Single step input used in conjunction with the SYNC output to step the program through each instruction (EPROM). This should be tied to +5V when not used. This pin is also used to put the device in Sync Mode by applying 12.5V to it.
$\overline{\text{CS}}$	7	I	CHIP SELECT: Chip select input used to select one UPI microcomputer out of several connected to a common data bus.
EA	9	I	EXTERNAL ACCESS: External access input which allows emulation, testing and ROM/EPROM verification. This pin should be tied low if unused.
$\overline{\text{RD}}$	9	I	READ: I/O read input which enables the master CPU to read data and status words from the OUTPUT DATA BUS BUFFER or status register.
A0	10	I	COMMAND/DATA SELECT: Address Input used by the master processor to indicate whether byte transfer is data (A0=0, F1 is reset) or command (A0=1, F1 is set). A0=0 during program and verify operations.
/WR	11	I	WRITE: I/O write input which enables the master CPU to write data and command words to the UPI INPUT DATA BUS BUFFER.
SYNC	13	O	OUTPUT CLOCK: Output signal which occurs once per UPI istruction cycle. SYNC can be used as a strobe for external circuitry; it is also used to synchronize single step operation.
D0-D7 (BUS)	14-21	I/O	DATA BUS: Three-state, bidirectional DATA BUS BUFFER lines used to interface the UPI microcomputer to an 8-bit master system data bus.
P10-P17	30-33 35-38	I/O	PORT 1: 8-bit, PORT 1 quasi-bidirectional I/O lines. P10-P17 access the signature row and security bit.
P20-P27	24-27 39-42	I/O	PORT 2: 8-bit, PORT 2 quasi-bidirectional I/O lines.The lower 4 bits (P20-P23) interface directly to the 8243 I/O expander device and contain address and data information during PORT 4-7 access. The upper 4 bits (P24-P27) can be programmed to provide interrupt Request and DMA Handshake capability. Software control can configure P24 as Output Buffer Full (OBF) interrupt, P25 as Input Buffer Full (/IBF) interrupt, P26 as DMA Request (DRQ), and P27 as DMA ACKnowledge (/DACK).
PROG	28	I/O	PROGRAM: Multifunction pin used as the program pulse input during PROM programming. During I/O expander access the PROG pin acts as an address/data strobe to the 8243. This pin should be tied high if unused.
VCC	44		POWER: +5V main power supply pin.

Symbol	Pin	Type	Description
VDD	29		POWER: +5V during normal operation. +12.5V during programming operation. Low power standby supply pin.
VSS	22		GROUND: Circuit ground potential.

(2) Absolute Maximum Ratings

Ambient Temperature Under Bias	0°C to + 70°C
Storage Temperature	-65°C to + 150°C
Voltage on Any Pin with Respect to Ground	-0.5V to + 7V
Power Dissipation	1.5W

7-2. N8042PC Keyboard Controller

The N8042PC is a general-purpose Universal Peripheral Interface that allows designer to develop customized solutions for peripheral device control.
The N8042PC is programmed with Phoenix Technologies Ltd. keyboard controller firmware (Phoenix MultiKey/42) for AT-compatible systems.

7-3. Phoenix MultiKey/42 Firmware

(1) Overview

Phoenix MultiKey/42 is designed to function as keyboard controller firmware in any AT or PS/2 compatible PC systems. MultiKey/42 is self-configuring and can function in different IBM-compatible
platforms at varying speeds without any changes to the code or hardware.

(2) Features

MultiKey/42 features and functionality include:

* AT and PS/2 Environment Autosensing.
* Support for AT, EISA and MC environments.
* New code base for high performance and optimized flexible structure.
* Support for keyboard controller-intensive applications such as Novell Netware.
* PS/2 style mouse support as standard feature.
* Password as standard feature.
* Keylock as standard feature.
* Speed-Independent Operation.

(3) Firmware

MultiKey keyboard BIOS from Phoenix allows the 8042 family of microcontrollers to operate as a keyboard controller in personal computers, including new small form factor PCs. The system firmware involved in keyboard integration includes a Keyboard Controller (KBC).
Keyboard Controller (KBC) is a hardware/software combination that interprets keyboard scan codes and serves as an interface between the keyboard subsystem and the rest of the computer. The KBC also controls auxiliary devices such as the mouse and other input devices. In addition, various pieces of the KBC hardware and software can be used for unrelated functions. For example, it is common in AT compatible machines to use the keyboard controller to provide speed switching capability. The KBC also controls GateA20 and system reset lines.
Environmental Autosensing - Once the local wiring diagram is detected, MultiKey/42 responds solely as an AT 8042 or PS/2 8042. A manufacturer need only stock one part to work with their full line of system products.

MultiKey/42 preforms several tests to identify the environment in which the 8042 is connected (AT, PS/2 or AT with mouse). MultiKey/42 uses the looped back interface lines to detect the environment type. Since the auxiliary device interface line can be connected to various unknown hardware in an AT environment, the only sure line to test is the Keyboard Data line. Between the two environments, the keyboard data line is inverted and connected to different inputs on the 8042.
Improved GateA20 Support for keyboard controller-intensive applications. These are applications that issue so many GateA20 commands that the 8042 can no longer perform its primary function, checking for keyboard or auxiliary device transmissions. The keyboard and auxiliary devices must be inhibited while the 8042 is processing commands, otherwise the transmissions will fail. Because there is no handshaking between the 8042 and the keyboard/auxiliary device, the main loop must check each device within 40us (about 8 instructions at 6MHz). The MultiKey/42 architecture allows the GateA20 command (D1h) to be processed without inhibiting the keyboard or auxiliary device interface. This permits uninterrupted typing when using keyboard controller-intensive applications that violate the 8042 interface.
Speed Independent Operation - Traditionally, system designers have used 8042 clock from 6MHz to 12 MHz. The MultiKey/42 uses timer loops based on the clock to determine transmission errors. The default time values, loaded in 8042 RAM, are set at 10MHz and can be changed by PhoenixBIOS. The 10MHz values operate efficiently in a 6-12MHz system. The IBM compatible values of RAM locations 27h to 29h for systems from 6-12MHz are shown below.

LOCATION	6MHz	8MHz	10MHz	12MHz
RAM27h (timer=380µs)	0FBh	0FAh	0F8h	0F6h
RAM28h (timer=2.40ms)	0E1h	0E1h	0D7h	0C4h
RAM29h (timer=11.8ms)	068h	068h	039h	000h

(4) Memory Map

RAM Location	Description
00h	(R0) Temp Register
01h	(R1) Temp Register
02h	(R2) 8042 Miscellaneous Flags
03h	(R3) 8042 State Flags
04h	(R4) Last Received Auxiliary Device Data
05h	(R5) Temp Register
06h	(R6) 8042 Timeout Flags
07h	(R7) Accumulator Storage
08h-17h	Program Stack
18h	Index for Phoenix Extended Memory Commands
19h	Keyboard State, ScanCode Set, LED Information
1Ah	Keyboard Typematic Delay & Rate Information
1Bh	Last Received Keyboard Data
1Ch-1Fh	Reserved
20h	Keyboard Controller Command Byte (KCCB)
21h	Number of Transmission Retries

RAM Location	Description
22h	Expect Keyboard Responses
23h	Number of Keyboard Resends
24h-26h	IBM Reserved
27h	380µs Timer Value
28h	2.4ms Timer Value
29h	11.8ms Timer Value
2Ah-2Ch	IBM Reserved
2Dh	ScanCode Break Flag
2Eh-2Fh	IBM Reserved
30h	Expect Auxiliary Device Responses
31h	Number of Auxiliary Device Resends
32h	IBM Reserved
33h	Password NULL1 Data
34h	Password NULL2 Data
35h	IBM Reserved
36h	Password Skip ScanCode1
37h	Password Skip ScanCode2
38h-3Fh	IBM Reserved
40h	Password Index
41h-49h	Password Area (9 bytes)
4Ah-7Fh	Reserved

(5) Status Register

Bit	AT	PS/2	Default	Description
7	X	X	0	Parity Error 1 = last byte received had incorrect parity.
6		X	0	General Timeout 1 = last transmission timed out before completion.
	X		0	Receive Timeout 1 = last transmission timed out before completion.
5		X	0	Auxiliary Device Output Buffer Full 1 = auxiliary output buffer contains data from the auxiliary device.
	X		0	Transmit Timeout 1 = last transmission timed out before completion.
4	X	X	0	Inhibited Switch 1 = the devices are uninhibited. This bit is cleared when password is enabled or if Port 1 bit7 = 0
3	X	X	1	Command/Data (F1) Set when system writes to Port 64h. Cleared when system writes to Port 60h.
2	X	X	1	System Flag (F0) Value = value of the system bit (bit3) in the Keyboard Controller Command Byte.
1	X	X	0	Input Buffer Full (IBF) 1 = input buffer contains data for the keyboard controller.
0	X	X	0	Output Buffer Full (OBF) 1 = output buffer contains data for the system.

(6) MultiKey/42 Standard Command Set

The AT compatible of MultiKey/42 includes support for several of the PS/2 commands that are not supported by the IBM AT standard. The following table lists the standard commands and indicates which commands are implemented in MultiKey/42 for AT and PS/2.

Address	AT	PS/2	Description
00h-1Fh	X	X	Read the contents of the designated RAM locations (20h-3Fh) and send it to the system.
20h-3Fh	X	X	Read from RAM.
40h-5Fh	X	X	Get a byte of data from system and write into one of location (20h-3Fh).
60h-7Fh	X	X	Write to RAM.
A4h	X	X	Test Password. Returns 0FAh if password is loaded. Returns 0F1h if password is not loaded.
A5h	X	X	Load Password. Loads password until a '0' is received from the system.
A6h	X	X	Enable Password. Enables the checking of keystrokes for a match with the password.
A7h		X	Disable Auxiliary Device.
A8h		X	Enable Auxiliary Device.
A9h		X	Test Auxiliary Device Clock and Data.
AAh	X	X	8051 Self Test. Returns 055h if successful self test.
ABh	X	X	Test Keyboard Clock and Data lines.
ACh			The Diagnostic Dump is not implemented.
ADh	X	X	Disable Keyboard.
AEh	X	X	Enable Keyboard
C0h	X	X	Emulate reading the input port (P1) and send data to the system.
C1h		X	Continuously puts the lower four bits of Port 1 into the STATUS register.
C2h		X	Continuously puts the upper four bits of Port 1 into the STATUS register.
D0h	X	X	Send Port 2 value to the system (emulates data since there's no real P2).
D1h	X	X	Only set/reset GateA20 line based on the system data bit 1.
D2h	X	X	Send data back to the system as if it came from the keyboard.
D3h		X	Send data back to the system as if it came from the auxiliary device.
D4h		X	Output next received byte of data from system to auxiliary device.
E0h	X	X	Reports the state of the test inputs. Phoenix BIOS requires the response to equal 00h on a PS/2, but with an XT keyboard attached the interface is set to 01h. Therefore, when an XT keyboard is attached, the response is forced to equal 00h.
FXh	X	X	Pulse only P2.0 (the reset line) low for 6µs if Command byte is even.

(7) MultiKey/42 Extended Command Set

Address	AT	PS/2	Description
B8h	X	X	Setup Phoenix extended memory access INDEX.
B9h	X	X	Get current Phoenix extended memory access INDEX.
BAh	X	X	Get current Phoenix extended memory referenced by INDEX.
BBh	X	X	Write Phoenix extended memory referenced by INDEX.
BCh-BDh	X	X	Read/Write RAM @VPointer Translates Phoenix extended index to 18 interesting memory locations, supportable on different memory or processor environments KCCB (0) Keyboard Controller Command Byte KCSTATE (1) Keyboard Controller State flags KCMISC (2) Keyboard Controller Misc flags TMRATE1 (3) 380µs for device to take 1 bit TMRATE2 (4) 2.4ms to receive a byte of data TMRATE3 (5) 12.0ms for device to receive first bit PWSTART (6) Start of Password area PWINDEX (7) Password index KSTATE1 (8) Keyboard Scan Code Set and LED state KSTATE2 (9) Keyboard Typematic Delay and Rate
C7h	X	X	Sets Port 1 bits corresponding bits to system data bits that are set.
C8h	X	X	Clears Port 1 bits corresponding bits to system data bits that are set.
C9h	X	X	Sets Port 2 bits corresponding bits to system data bits that are set.
CAh	X	X	Clears Port 2 bits corresponding bits to system data bits that are set.
D3h-D4h	X		Set/Clear Fast GateA20. Acknowledge (0FAh) is sent to the system upon completion of the command.
D5h	X	X	Read Phoenix Version Number (2 bytes). Send Version number (2 bytes). The digits (CONVERT filled) are in BCD format (version 2.48.11) and is stored as 24,8B and sent to the system in that order.
D6h	X	X	Read Version Information (2 bytes). Byte 1 — Byte 2 bit7 8042 Type processor Flip/Flop — bit7 IRQ12 Software bit6 XT Keyboard support inverted — bit6 IRQ12 Software bit5 Keyboard scanning support — bit5 IRQ1 Software Flip/Flop bit4 Intr. driven architecture inverted — bit4 IRQ1 Software bit3 Customized MultiKey speed,bit3 — bit3 8042 Clock bit2 Reserved — bit2 8042 Clock speed,bit3 bit1 AT Environment (0=PS/2) — bit1 8042 Clock speed,bit1 it0 AT Type keyboard (0=XT) — bit0 8042 Clock speed,bit0
D7h	X	X	Read Model number (2 bytes) and then read the customer's model number (1 byte).
D8h-D9h	X	X	Set/Clear Fast GateA20. Acknowledge (0FAh) is sent to the system upon completion of the command.
EXh	X	X	The Phoenix extended 0dd EXh commands sets P2.1, 2 or 3 based on command bits 1, 2 and 3. Even EXh commands clears P2.1, 2 or 3 based on command bits 1, 2 and 3.

(8) Keyboard Controller Command Byte

The internal status is defined by the Keyboard Controller Command Byte (KCCB). The KCCB resides in RAM at location 20h. The KCCB can be read/written with the special commands listed below.

Note: The KCCB is read with a 20h command and written with a 60h command.

Bit	AT	PS/2	Default	Description
7	X	X	0	Reserved = 0
6	X	X	1	IBM PC Compatibility Mode 1 = translate scan codes to IBM PC standard before passing to the system. 0 = pass untranslated scan codes to the system.
5		X	1	Disable Auxiliary Device 1 = auxiliary device disabled (interface inactive)
	X		0	IBM PC Mode 1 = XT keyboard support
4	X	X	0	Disable Keyboard 1 = keyboard disabled (interface inactive)
3		X	0	Reserved = 0
	X		0	Inhibit Override 1= disable keyboard inhibit function
2	X	X	1	System Flag 1 = the system is executing POST as a result of a shutdown or warm boot. 0 = the system is executing POST as a result of a cold boot. Note: The value of this bit is written to the system flag bit of the status register (bit2 of a read of Port 64h).
1		X	0	Enable Auxiliary Output Buffer Full Interrupt. 1 = an interrupt to system is generated when a byte is placed into the auxiliary output buffer (port2, bit5 set to 1).
	X		0	Reserved
0	X	X	0	Enable Keyboard Output Buffer Full Interrupt 1 = an interrupt to system is generated when a byte is placed into the output buffer (port2, bit4 set to 1).

(9) Keyboard Command

Any command/data written to Port 60h is automatically transmitted to the keyboard by the 8042 if MultiKey/42 is not in a waiting-for-data mode. In the case of a two-byte keyboard command, for example
Set LEDs (0EDh), both the command and data are written to Port 60h.

Command (Hex)	Description
ED	Set LEDs
EE	Echo
EF	Invalid command
F0	Select alternate scan code set
F1	Invalid command
F2	Read ID bytes
F3	Set typematic delay and rate
F4	Enable keyboard
F5	Disable keyboard and set defaults
F6	Set defaults
F7*	Set all keys typematic

Command (Hex)	Description
F8*	Set all keys make/break
F9*	Set all keys make only
FA*	Set all keys typematic/make/break
FB*	Set key type typematic
FC*	Set key type make/break
FD*	Set key type make only
FE	Resend the last transmission
FF	BAT, reset the defaults and buffers

*Commands F7 through FD are normally used for Character Set 3

(10) Auxiliary Device Command

The Auxiliary Device command sequence is as follows:

1. Write an 8042 command D4h (Write Auxiliary Device) to Port 64h.
2. Write Command/data to Port 60h.

The above sequence is executed twice for two-byte Auxiliary Device commands, such as the Set Scaling (0E7h) command.

Command (Hex)	Description
E6h	Reset Scaling
E7h	Set Scaling
E8h	Set Resolution
E9h	Status Request
EAh	Set Stream Mode
EBh	Read Data
ECh	Reset Wrap Mode
EDh	Invalid Command
EEh	Set Wrap Mode
EFh	Invalid Command
F0h	Set Remote Mode
F1h	Invalid Command
F2h	Read Device Type
F3h	Set Sampling Rate
F4h	Enable Auxiliary Device
F5h	Disable Auxiliary Device
F6h	Set Default Values
F7h - FDh	Reserved
FEh	Resend
FFh	Reset

8. V9LP Keyboard Encoder

8-1. Overiew

PARES V9LP is a single chip, SMT TYPE, PLCC 44pins, CMOS microprocessor-based keyboard encoder, it is used for building an IBM PC family compatible keyboard and a NOTEBOOK PC keyboard or an numericKEY-PAD of notebook PC, it incorporate with all of the standard functions of IBM PC AT, PS2 101/102 KEYS keyboard and the special functions for NOTEBOOK PC that derive from the standard.

PAREX-V9LP encoder features:

- Very low power consumption typical 1-10 uA @ 5V.
- Wide range operation voltage 3-6V.
- Supports standard external keyboard and keypad interface that enable the inner K.B. With external K.B. or keypad works simoultaneously.
- Three control outputs, for suspend sleeping output, power down output and backlight on/off control.
- Programmable power down.
- Numeric keys convert, function key convert.
- Hot key.
- Keylock (pass word) security.
- Digitize trimmer for LCD brightness and contrast controll.
- Multimatrix for OKI.
- support DOS-V Japan/Chinese system.
- PLCC pakage.

8-2. Pin Diagram

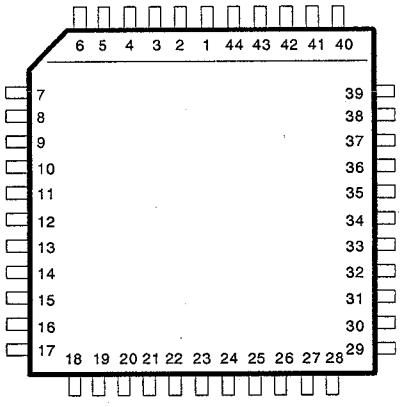


Fig. 4-11: V9LP Pin Diagram

8-3. Pin Assignment

Pin	Signal	Description
1	B5	Output, Scanning xE.
2	B7	Output, Scanning xF, Brightness Chip Select.
3	B0	Output, Scanning xA.
4	B1	Output, Scanning x9, Scrolllock Indicator Dreive.
5	B2	Output, Scanning x8, Num Lock Indicator Drive.
6	NC	
7	A0	Input, Scanning y7.
8	A1	Input, Scanning y6.
9	A2	Input, Scanning y5.
10	A3	Input, Scanning y4.
11	A4	Input, Scanning y3.
12	A7	Input, Scanning y2.
13	IT3	Input, External Keyboard Sense Input.
14	IT0	key press sense.
15	RES	Input, NMI reset, 50us low mininum.
16	A6	Input, Scanning y1.
17	NC	
18	A5	input, scanning y0.
19 20	OSC1 OSC2	Input, R-C Circuit, to be Runing at 5 Mhz.
21	D7	Bidirection, scanning x7. OKI matrix select.
22	D6	Bidirection, Scanning x8.
23	Vss	Input, Gnd +0 / -0 V.
24	D5	Bidirection, Scanning x5.
25	D4	Bidirection, Scanning x4.
26	D3	Bidirection, Scanning x3.
27	D2	Bidirection, Scanning x2.
28	Vcc	Input, Vcc + 3.0 - 6V
29	D1	Bidrection, Scanning X1 Output.
30	D0	Bidrection, scanning x0 output, suspend notice input.
		Bidrection, scanning x0 output, suspend notice input. this pin also used as suspend notice input, when system falling suspend, will issue a suspend notice (low active) to this pin and will issue a SMI signal when press space-bar key lonly.
31 32	EKBDATA EKBCLK	Bidirection, external keyboard/ key pad data. directly apply to external clk, data line, shall equip with a maximum value - 10k ohms pull high resister.
33	C2	This pin is an ouput, will drive low after press FN + Del for power down purpose. and will goes high after press Fn + space for POWER ON.
34	SMI	SMI output, produce a pulse when press HOT keys. it will issue a SMI pulse and a hardware hot key value. the HOT key are: FN+S FN+f3 FN+f4 FN+f5 Fn+Esc Fn+!1 Fn+@2 and Fn+B.
35	C4	Toggle output, press Fn+F6 toggle this output, normal high when first apply power.
36	Func	Output, Drive Low Output. Brightness, Contrast Latch Clock Pulse.
37	DATA	Bidirection, Interface To System, Data Line.
38	CLOCK	Bidirection, Interface To System, Clock Line.
39	Vss	Input, Gnd + 0 / -0 V.
40	Vss	Input, Gnd + 0 / -0 V.
41	B3	Output, Scanning XB, Caps Lock Indicator Drive.
42	B4	Output, Scanning xC.
43	B6	Output, Scanning xD. Contrast Chip Select.
44	Vss	Input, Gnd + 0 / -0 V.

8-4. Function Description

(1) FN-key functions

The Fn key is a function alternative key, it is used for combinating other keys to produce special key functions.

(2) Fn with F1, F2

Fn+F1=F11, Fn+F2=F12

(3) Fn with F3, F4, F5, F6, F7, F8, F9, F10

When preess the following HOT key, that produce 50 + 70/-20 ms SMI pulse, with the value.

	PB02	PB01	PB00
Fn+S	0	0	0
Fn+F4	0	0	1
Fn+F5	0	1	0
Fn+B	0	1	1
Fn+F3	1	0	0
Fn+Esc	1	0	1
Fn+1	1	1	0
Fn+2	1	1	1

a Fn + S or a suspend notice will cause the encoder enter suspend mode and a key press "space bar" will introduce a SMI pulse again.

(4) Fn with F6 for backlight on/off.

Press Fn with F6, will cause the ouput pin C4 to toggle from high to low, or from low to high.

(5) Digitized brightness controll

pressing Fn + F8 increase the output value of brightness latch. Fn + F7 decrease the value.

(6) Digitized contrast controll

pressing Fn + F9 increase the output value of contrast latch. Fn + F10 decrese the value.

(7) Fn with cursor move key, up arrow, down arrow, left arrow, right arrow.

Fn + up arrow =PgUp
Fn + down arrow =PgDn
Fn + left arrow =Home
Fn + right arrow =End

(8) Fn with PgUp PgDn Home END

Fn +
PgUp
PgDn
Home
End
=
Home
End
End
Home

These are for DOS-V Japan keyboard purpose
Fn with del will cause the output of C2 to low, and press Fn + space to make C2 to high.

(9) Fn with Ins

pressing Fn + Ins = rightward Ctr1.

(10) Fn with capslock – key lock

Press Fn+capslock cause the keyboard enter keylock status, only the password BEE typied in, then the keyboard activated. Due to this keyboard encoder, its Icc typically take about 1 to 10 ua, that is possible to apply the power (say RTC) to its all -the time, therefore it's useful to install this keylock function. in general, this keylock are like the password function in the bios, the only special is "You can make the Notebook PC enter keylock (into password check state at any time, it never care the PC is runing under which envirments, because it is fully independent from system. that means if the system "under running a pakage", the user can type FN+caplock to disable key-in execpt the password).
the keylock function is performed by system sending a "pass ward" to keyboard with "EF" command, after "EF" command, the first byte is command byte, the definition are first byte second byte pass wordEF 10 .....set password and activate keylock function, but not falling key lock state. EF 20 read pass word back to system. EF 30 set keylock, enter keylock state, only the pass word be keyin, or anEF 40 be send to keyboard, then the keyboard be activated again. FE 40 release keylock instead of key in pass word from keyboard.
press Fn + Caps lock = key lock
set password to keyboard only function diode "ENBEF" be install, the encoder then be enabled to receive "EF" command and its password data byte, and only sending password to the encoder, the encoder then be enabled to accept and enter keylock state by pressing Fn+Caps lock, otherwise the keylock function is initially disable.
to set password, first check to install the diode "ENBEF", then sending "EF" "10" to encoder from system, after EF10, the following is pass word, could be any length, but maximum 15 bytes, and follow a end delemeter code "77", the bit 7 of each byte of pass word must be always "0".
after power on or "FF" command, the pass word have to load again.
Only the password is loaded to Keyboard encoder, then enable FN+caslock, otherwise doing nothing aftter press Fn+capslock.

(11) NUM LOCK Key Functions

the Num-Lock Key is a toggle key, be pressed to Lock the UIO group to number key, or to release lock from number key back to UIO group.

key legend	& 7	* 8	(9	U	I	O	J	K	L	M	> .	? /	: ;	P	) 0
NUM LOCK (ON)	7 Ho me	8 I	9 Pg Up	4	5	6	1 End	2 I	3 Pg Dn	0 Ins	. Del	/	+	-	*
NUM LOCK (OFF) release	& 7	* 8	(9	U	I	O	J	K	L	M	.	? /	: ;	P	) 0

The Return key converted to Enter key while NUM (PAD) LOCK on.

(12) Fn with UIO group

Fn wiht &7, *8, (9, U, I, O, J, K, L, M, ., ?/, P,)0, {[, }].
The group of &7, *8, (9, U, I, O, J, K, L, M, ., ?/, P,)0, {[, }] is known as UIO NUMERIC group, normally, in the case of UNM (PAD) LOCK off and no Fn key be hold, the keys of this group functionsas it legend shown.
Depending on the NUM (PAD) lock ON or OFF, pressing FN key first and hold, then the keys of the group, the function responsed as the table below shown.

key legend	& 7	* 8	(9	U	I	O	J	K	L	M	> .	? /	: ;	P	) 0
Fn Key and NUM LOCK off	7 Ho me	8 I	9 Pg Up	4	5	6	1 End	2 I	3 Pg Dn	0 Ins	. Del	/ /	+ +	- -	* *
Fn Key and NUM LOCK on	& 7	* 8	(9	U	I	O	J	K	L	M	> .	? /	: ;	P	) 0

Fn with return key, produce return while Num (PAD) lock on, produce ENTER while Num (PAD) Lock off.

(13) other associated with Fn key

A combination of Fn key with two FN-associated key be pressed simoutanuously, only the key directly follow the Fn is converted.
If pressing Fn key first and hold then pressing left side Ctrl or Alt and hold then any key of UIO group, the keys of UIO group will don't affected (converted) by Fn key, it just depending on eitherNUM (PAD) LOCK on or off.
If pressing and hold Ctrl and Alt key first, then pressing Fn key and then the keys of UIO group, the keys of UIO group will affected by Fn key.

(14) Support DOS-V key matrix

V9LP have equip with 5 extra keymatrix for 5 extra keys of DOS-V to produce code: 6A 51 67 64 13 for japaness keyboard.

(15) External keyboard interface

The external keyboard interface support to IBM standard or its fully compatible keyboad.
the inner keyboard received keycodes from external keyboard or keypad, and pass to system, and acknowlage command from system and pass to external keyboard or keypad. this makes the inner keyboardworks with external keyboard or keypad simoultaneously.
After external keyboard be plung in, the encoder autodisable the UIO group to convert to numberic keypad.

(16) Four LED drivers

Four LED indictors for
1.Caps Lock.
2.Scroll Lock.
3.Num Lock.
4.Key lock.

8-5. Programming Command

The V9LP can be programmed through key board intaface. Be sides standand Command of AT Compatible machine, V9LP supports additional commands to control keyboard and power management pins. The Commands
are always start with a "F1" code. Then an action code. They are shown as followed:

F1 00 FN+DEL FUNCTION DISABLE

F1 01 ENABLE FN+DEL FUNCTION

F1 02 SELECT OKI MTX

F1 03 DIRECT CAUSE C4 (BACKLIGHT CONTROL PIN) TO HIGH

F1 04 DIRECT CAUSE C4 TO LOW

F1 05 READ LED STATUS TO SYSTEM

F1 06 READ BR/CT STATUS TO SYSTEM

F1 07 WRITE BR/CT FROM SYSTEM

F1 08 SELECT IBM MTX

F1 0D READ VERSION NUMBER

F1 0E select Chaplet hot key.

F1 0F DIRECT CAUSE POWER DOWN, C2 TO LOW

F1 10 =5.6ms / STEP, PROGRAM CONTRACT, BRIGHTNESS COUNTER SPEED

F1 11 =11.2ms / STEP, AND SO ON ....., UP TO "F1 7F"

9. TH6460B Super Multi-I/O Chip

(1) Pin Diagram

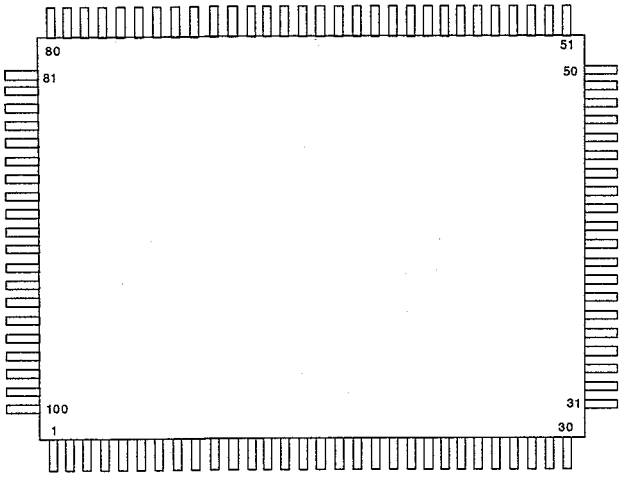


Fig. 4-12: TH6460B Pin Diagram

(2) Pin Description

Pin	Symbol	Type	Description
1	SA9	I	System Address bus 9.
2	SA8	I	System Address bus 8.
3	SA7	I	System Address bus 7.
4	SA6	I	System Address bus 6.
5	SA5	I	System Address bus 5.
6	SA4	I	System Address bus 4.
7	SA3	I	System Address bus 3.
8	SA2	I	System Address bus 2.
9	SA1	I	System Address bus 1.
10	SA0	I	System Address bus 0.
11	AEN	I	Address Enable.
12	RESET	I	System reset.
13	$\overline{MO1}$	O	FDD Motor 1 enable.
14	$\overline{MO0}$	O	FDD Motor 0 enable.
15	VSS		Ground.
16	$\overline{GMWR}$	O	Game port Write.
17	/GMRD ATXTZ	O	Game port Read. During system reset, it is the input to setup AT ot XT mode. AT mode is selected when ATXTZ=1.
18	PD7	O	Printer Data 7.
19	PD6	O	Printer Data 6.
20	PD5	O	Printer Data 5.
21	PD4 $\overline{EXDCHG}$	I/O	In external printer mode, this pin is Printer Data 4. In external floppy mode, this pin is FDD Disk Change.
22	VDD	I	+5V.
23	VSS		Ground.
24	PD3 $\overline{EXTR0}$	I/O	In external printer mode, this pin is Printer Data 3. In external floppy mode, this pin is FDD Track0 detect.
25	PD2 $\overline{EXWP}$	I/O	In external printer mode, this pin is Printer Data 2. In external floppy mode, this pin is FDD Write Protect.
26	PD1 $\overline{EXRDD}$	I/O	In external printer mode, this pin is Printer Data 1. In external floppy mode, this pin is FDD Read Data.
27	PD0 $\overline{EXIDX}$	I/O	In external printer mode, this pin is Printer Data 0. In external floppy mode, this pin is FDD Index Detect.
28	$\overline{ERROR}$	I	Printer Error.
29	SLCT	I	Printer Select.
30	PE	I	Paper End.
31	$\overline{ACK}$	I	Printer Acknowledge.
32	BUSY	I	Printer Busy.
33	$\overline{STROBE}$	I/O	Printer Strobe.
34	$\overline{AUTOFD}$	I/O	Printer Autofeed.
35	$\overline{INIT}$	I/O	Printer Initiate.

Pin	Symbol	Type	Description
36	$\overline{\text{SLCTIN}}$	I/O	Select Input.
37	SOUTB PRSEL1	I/O	In normal operation, this pin is COM B data Output. During system reset, it is the input to setup configuration register 2 bit7.
38	$\overline{\text{DTRB}}$ DISFDC	I/O	In normal operation, this pin is COM B Data Terminal Ready. During system reset, it is the input to setup configuration register 2 bit3. FDC is Disabled when it equals 1 and enabled when it equals 0.
39	/RTSB PRSEL0	I/O	In normal operation, this pin is COM B Request To Send. During system reset, it is the input to setup configuration register 2 bit6.
40	VDD	I	+5V.
41	VSS		Ground.
42	SD7	I/O	System Data bus 7.
43	SD6	I/O	System Data bus 6.
44	SD5	I/O	System Data bus 5.
45	SD4	I/O	System Data bus 4.
46	SINB	I	COM B data Input.
47	$\overline{\text{DSRB}}$	I	COM B Data Set Ready.
48	$\overline{\text{DCDB}}$	I	COM B Data Carrier Detect.
49	$\overline{\text{CTSB}}$	I	COM B Clear To Send.
50	$\overline{\text{RIB}}$	I	COM B Ring Indicator.
51	$\overline{\text{RIA}}$	I	COM A Ring Indicator.
52	$\overline{\text{CTSA}}$	I	COM A Clear To Send.
53	$\overline{\text{DCDA}}$	I	COM A Data Carrier Detect.
54	$\overline{\text{DSRA}}$	I	COM A Data Set Ready.
55	SINA	I	COM A data Input.
56	$\overline{\text{RTSA}}$ DISCOMB	I/O	In normal operation, this pin is COM A Request To Send. During system reset, it is the input to setup configuration register 2 bit2. COM B is disabled when it equals 1 and enabled when it equals 0.
57	$\overline{\text{DTRA}}$ COMSEL	I/O	In normal operation, this pin is COM A Data Terminal Ready. During system reset, it is the input to setup configuration register 2 bit0. COM1 and COM2 is selcted when it equals 1 and COM3 and COM4 is selected when it equals 0.
58	SOUTA DISCOMA	I/O	In normal operation, this pin is COM A data Output. During system reset, it is the input to setup configuration register 2 bit1. COM A is disabled when it equals 1 and enabled when it equals 0.
59	SD0	I/O	System Data bus 0.
60	SD1	I/O	System Data bus 1.
61	SD2	I/O	System Data bus 2.
62	SD3	I/O	System Data bus 3.
63	VSS		Ground.
64	VDD	I	+5V.
65	DRQ2	O	FDC DMA Request.
66	IRQ3	O	COM2 or COM4 Interrupt Request.
67	IRQ4	O	COM1 or COM3 Interrupt Request.
68	IRQ5	O	Printer adapter (LPT2) Interrupt Request.
69	IRQ6	O	FDC Interrupt request.

Pin	Symbol	Type	Description
70	IRQ7	O	Printer adapter (LPT1 or LPT3) Interrupt Request.
71	$\overline{\text{CS0}}$ DISHDC	I/O	In normal operation, when AT mode is selected, it is HD /CS0. During system reset, it is the input to setup configuration register 2 bit4. HDC is disabled when it equals 1 and enabled when it equals 0.
72	$\overline{\text{CS1}}$ FDPR	I/O	In normal operation, when AT mode is selected, it is HD/CS1. During system reset, it is the input to setup configuration register 1 bit0. External floppy is selected when it equals 0 and external printer is selected when it equals 1.
73	HD7	O	In AT mode, this pin is HD data 7.
74	VSS		Ground.
75	$\overline{\text{WD}}$	O	FDD Write Data.
76	$\overline{\text{STEP}}$	O	FDD step.
77	OUT1 IN1	I/O	Configuration register 1 bit1. During system reset, it is the input to setup configuration register 1 bit1.
78	OUT2 IN2	I/O	Configuration register 1 bit2. During system reset, it is the input to setup configuration register 1 bit2.
79	$\overline{\text{HDCS}}$ DISGAME	I/O	In normal operation, when AT mode is selected, it is /HDCS. During system reset, it is the input to setup configuration register 2 bit5. Game port is disabled when it equals 1 and enabled when it equals 0.
80	$\overline{\text{EXFD}}$	I/O	Select External Floppy when it equals 0 and select external printer when it equals 1.
81	$\overline{\text{HDRES}}$	I	HD/RESET.
82	$\overline{\text{DACK2}}$	I	FDC DMA Acknowledge.
83	TC	I	FDC Terminal Count.
84	$\overline{\text{RDD}}$	O	FDD Read Data.
85	$\overline{\text{WE}}$	O	FDD Write Enable.
86	VDD	I	+5V.
87	OSCA	I	24MHz OSC input.
88	OSCB	O	24MHz OSC output.
89	$\overline{\text{DIRC}}$	O	FDD Direction.
90	$\overline{\text{DS1}}$	O	FDD Drive 1 enable.
91	VSS		Ground.
92	$\overline{\text{DS0}}$	O	FDD Drive 0 enable.
93	$\overline{\text{RWC}}$	O	FDD Reduce Write Current.
94	$\overline{\text{HS}}$	O	FDD Head Select.
95	$\overline{\text{IOR}}$	I	I/O Read.
96	$\overline{\text{IOW}}$	I	I/O Write.
97	$\overline{\text{TR0}}$	I	FDD Track0 detect.
98	$\overline{\text{IDX}}$	I	FDD Index Detect.
99	$\overline{\text{WP}}$	I	FDD Write Protect.
100	$\overline{\text{DCHG}}$	I	FDD Disk Change.

9-1. FDD Controller

In the TH6460, there is an FDC765A, Digital Data Separator, Write Precompensation and two FDC Peripheral Registers. It supports up to two floppy disk drivers. It is capable of either FM of MFM (includingdouble sided) recording, and will operate in either DMA or non-DMA mode.
In the non-DMA mode, the FDC generates an interrupt to the processor every time a data byte is to be transferred.
In DMA mode, the processor needs only to load the command into the FDC and all data transfers occur under the control of the FDC and DMA controllers respectively.
Pins of /MO0, /MO1, /DS0 and /DS1 control which disk drive is selected and which motor is enabled, and these 4 pins are controlled by port $3F2. Port $3F7 is used to set up the data transfer rate to250kB/s, 300kB/s or 500kB/s.

(1) Data Transfer Rate

Disk Drive	360kB	1.2MB		720kB	1.44MB	
Diskette	360kB	360kB	1.2MB	720kB	720kB	1.44MB
Data Transfer rate	250kB/s	300kB/s	500kB/s	250kB/s	300kB/s	500kB/s

(2) FDC Registers

The are four registers used by the FDC and their functions are described in the following table.

Address Decoder		Data	Application (PC XT/AT)
Function	Port		
$\overline{IOW}$	$3F2	XD0 XD1 XD2 XD3 XD4 XD5 XD6 XD7	0-DRV:1-DRV1Reserved /Controller Reset INT/DRQ enabled Motor 0 enabled Motor 1 enabled Reserved Reserved
$\overline{IOR}$	$3F4		Decoded for 765A main Status Register
$\overline{IOR}$, $\overline{IOW}$	$3F5		Decoded for 765A Data Register
$\overline{IOR}$	$3F7	XD0-XD6 XD7	Reserved Diskette Change
$\overline{IOW}$	$3F7	XD0 XD1 XD2-XD7	0 1 0 0 0 1 Trans. rate 500 300 250 Reserved

For example, if write data #01h is written to port $3F7, then 300kB/s transfer rate will be selected. There is a built-in FDC 765A which executes 15 commands.
Port $3F4 and port $3F5 are decoded for 765A main status register (MSR) and data register (DR). The MSR contains the status information of the FDC, and may be accessed at any time.
The DR (which actually consists of several registers in a stack with only one register presented to the data bus at a time) stores data commands, parameters and FDD status information. Data bytes areread out of or written into the DR in order to program or obtain the results after a particular command. Therefore users can program FDC 765A via port $3F4 and $3F5.
TH6460 supports 24mA flexible driver interface buffers. Therefore, all the FDD control pins will connect to the FDD connector directly.

(3) Internal FDD Connector Pin Assignment

Pin	Symbol	Type	Description
1	VDD		+5v
2	$\overline{IDX}$	I	Index detect
3	VDD		+5V
4	$\overline{DS0}$	O	Drive 0 enabled
5	N.C.		No connection
6	$\overline{DCHG}$	I	Disk change
7	N.C.		No connection
8	GND		Ground
9	N.C.		No connection
10	$\overline{MO0}$	O	Motor 0 enabled
11	N.C.		No connection
12	$\overline{DIRC}$	O	Direction
13	GND.		Ground
14	$\overline{STEP}$	O	FDD step
15	GND		Ground
16	$\overline{WD}$	O	Write data
17	GND		Ground
18	/WE	O	Write enabled
19	GND		Ground
20	$\overline{TR0}$	I	Track 0 detect
21	GND		Ground
22	$\overline{WP}$	I	Write protect
23	GND		Ground
24	$\overline{RDD}$	O	Read data
25	GND		Ground
26	$\overline{HS}$	O	Head select

Notes:

1. $\overline{\text{indicates}}$ active low signal. driection is with respect to the host.
2. I indicates to the host.
3. O indicates from the host.

9-2. Serial Communication Port 1

Description

There are two independent UARTs in the TH6460, and they are fully compatible with NS 16450. The UART performs serial-to-parallel conversion on data characters received from a peripheral device or a MODEM, and parallel-to-serial conversion on data characters received from the CPU. The CPU can read the complete status of the UART at any time during the operation.
Status information reported includes the type and condition of the transfer operations being performed by the UART, as well as any error conditions. In the TH6460, the programmable baud generator allows division of any input clock by 1 to generate the internal 16X clock.
There are eleven registers in each UART (as shown below). They can be accessed via the CPU. These registers control UART operations including transmission and reception of data.

(1) Serial Port Registers

DLAB (LCR bit7)	COM1 Port	Register Symbol	Register Name
0	$3F8	RBR	Receive Bufffer Register, Read Only
0	$3F8	THR	Transmitter Holding Register, Write Only
0	$3F9	IER	Interrupt Enable Register
0	$3FA	IIR	Interrupt Identification Register
X	$3FB	LCR	Line Control Register
X	$3FC	MCR	Modem Control Register
X	$3FD	LSR	Line Status Register
X	$3FE	MSR	Modem Status Register
X	$3FF	SCR	Scratch Status Register
1	$3F8	DLL	Divisor Register
1	$3F9	DLM	Divisor Registor

(2) Serial Port Connector Assignment

Pin	Symbol	Type	Description
1	$\overline{DCDA}$	I	Data carrier detect
2	SINA	I	Data input
3	SOITA	I/O	Data output
4	$\overline{DTRA}$	I/O	Data terminal ready
5	GEN		Signal ground
6	$\overline{DSRA}$	I	Data set ready
7	$\overline{RTSA}$	I/O	Request to send
8	$\overline{CTSA}$	I	Clear to send
9	$\overline{RIA}$	I	Ring indicate

Notes:

1. $\overline{\text{Indicates}}$ active low signal. Direction is with respect to the host.
2. I indicates to the host.
3. O indicates from the host.

9-3. Parallel Interface

(1) Printer Connector Pin Diagram

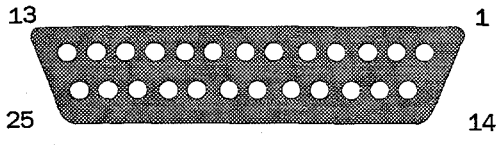


Fig. 4-13: Parallel Port

(2) Connector Pin Assignment

Pin	Symbol	Type	Description
1	$\overline{STROBE}$	I/O	Printer strobe
2	PDB 0	I/O	Print data bit 0
3	PDB 1	I/O	Print data bit 1
4	PDB 2	I/O	Print data bit 2
5	PDB 3	I/O	Print data bit 3
6	PDB 4	I/O	Print data bit 4
7	PDB 5	O	Print data bit 5
8	PDB 6	O	Print data bit 6
9	PDB 7	O	Print data bit 7
10	$\overline{ACKG}$	I	Printer acknowledge
11	BUSY	I	Printer busy
12	PE	I	Out of paper
13	SLCT	I/O	Printer select
14	$\overline{ATF}$	I/O	Auto feed
15	$\overline{ERROR}$	I	Printer error
16	/INIT	I/O	Initialize printer
17	$\overline{SLCTIN}$	I/O	Select input
18-25	GND		Ground

Notes:

1. $\overline{\text{Indicates}}$ active low signal. Direction is with respect to the host.
2. I indicates to the host.
3. O indicates from the host.

External FDD

The external FDD shares the same circuitry and connector interface as that of the parallel printer port. The signal $\overline{EXFD}$ at pin 80 of TH6460 helps to detect and select either external FDD or printer.

(3) External FDD Connector Pin Assignment

Pin	Symbol	Type	Description
1	N.C.		No connection
2	EXIDX	I	Index detect
3	EXTR0	I	Track 0 detect
4	EXWP	I	Write protect
5	EXRDD	O	Read data
6	EXDCHG	I	Disk change
7	N.C.		No connection
8	N.C.		No connection
9	N.C.		No connection
10	/DS1	O	Drive 1 enabled
11	MO1	O	Motor 1 enabled
12	WD	O	Write data
13	WE	O	Write enabled
14	RWC	O	Reduce write current
15	HS	O	Head select
16	DIRC	O	Direction
17	STEP	O	FDD step
18-24	GND		Ground
25	EXFD	I/O	FDD, when EXFD=0; PRN, when EXFD=1

Notes:

1. I indicates to the host.
2. O indicates from the host.

10. FDD Drive (Canon MD3671)

10-1. Description

The Canon MD3671, 3.5-inch micro floppy disk drive is activated by 5 voltage-single power source and provides 2MB and 1MB unformatted storage capacity respectively. Signal connection between MD3671 and the system are made via 26pin FFC connector.

(1) Key Feature

- Compact drive
  Canon MD3671 is only 12.7mm beight, 101.6mm width, 101.6mm depth and it weighs only 120g. Its compactness is suitable for use in lap top or note book size computer systems.
- Compact DD motor
  The compact DDmotor produced by Canon's precision machinery technology allows an extremely compact drive, and ensures high reliability.

10-2. SPECIFICATIONS

ITEMS \ MODE		2MB MODE	1MB MODE
Recording Capacity	Unformatted	2 MBytes	1MBytes
	Formatted	1474.6KbYTES	737.3KBytes
	Per Track	12.5KBytes	6.25KBytes
Data Transfer Rate		500 Kbits/sec.	250 Kbits/sec.
Recording Capacity Swiching System		Media Automatic Recognition.	
Access Time	Track to Track	3 msec. (min)	
	Seek Settling Time	15 msec.	
	Average Access Time	94 msec. (min)	
Disk Rotational Speed		300 rpm	
Average Latency		100 msec	
Spindle Motor Start Time		400 msec. (max)	
Recording Density at Innermost Track		1743 B.P.I.	8717 B.P.I.
Number of Tracks	Track Per Side	80	
	Track Per Disk	160	
Track Density		135 T.P.I.	
Number of Head		2	
Encoding Method		MFM	

Environmental Conditions	MODE / ITEMS	Operating	Non-operating	Transporting
	TEmperature	5°C45°C	-22°C55°C	-40°C62°C
	Humidity	20-80 %RH	10-90 %RH	5-90 %RH
	Maximum Wet Bulb Temperature	29°C	40°C	42°C

Vibration Resistance		0.5G	2G	2G
Shock Resistance		5G	100 G for 11 msec.	
D.C. Voltage Requirements		+5V±10%, Ripple; 100 mVp-p(DC to 1MHz)		
Power Consumption		Stand by ; 45 mW (TYP)		
		Operating ; 1.3 W (TYP)		
External View		12.7 mm(H)x101.6 mm(W)x101.6 (105.6)		
Weight		120 g (TYP)		
Bezel and Button Color		Black		
Activity LED		Green		
Reliability	MTBF	10,000 P.O.H		
	MTTR	30 min.		
	Unit Life	5 years		
	Soft Read Errors	Less than 10 -9 bits.		
	Hard Read Errors	Less than 10 -12 bits.		
	Seek Errors	Less than 10 -6 bits.		

10-3. INTERFACE

(1) Signal Interface

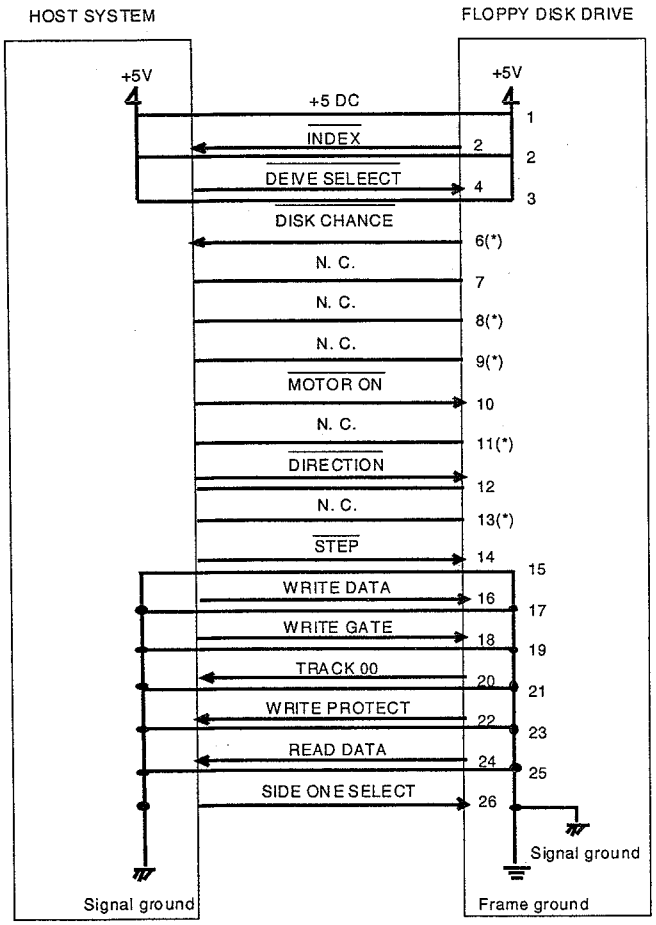


Fig. 4-14: Signal Interface

*Optional Signal Lines.
6 pin: DRIVE SELECT 1
8 pin: HD OUT or READY
9 pin: HD OUT
11pin: HD SEL. or LD SEL.
13 pin: DISK CHANGE or READY

11. Internal Key board (BTC-5004 Notebook keyboard)

11-1. Specification:

1. OUTSIDE DIMENSION: 278.45x114.8x10.2mm
2. KEY LAYOUT: SEE ATTACHED
3. TOTAL HEIGHT: 10.2 + /-0.2mm
4. KEY PITCH: 18.36mm
5. WEIGHT: 155 + /20g
6. SWITCH TYPE: CONDUCTIVE RUBBER
7. ACTUATION FORCE: 55 + /-15g
8. TRAVEL: 2.5 + /-0.2mm
9. CONTACT RESISTANCE: MAX 1kOHM
10. BOUNCE: MAX 15ms
11. LIFE: OVER 5 MILLION CYCLE
12. FN KEY
13. COMPATIBILITY: 85/86 KEY KEYBOARD COMPATIBLE WITH 101/102 AT AND PS/2 FUNCTION
14. KEYTOP LEGEND ENDURANCE: MEET CNS
15. EXTRACTION FORCE: 1.2g MIN.

(1) Key Position Numbers

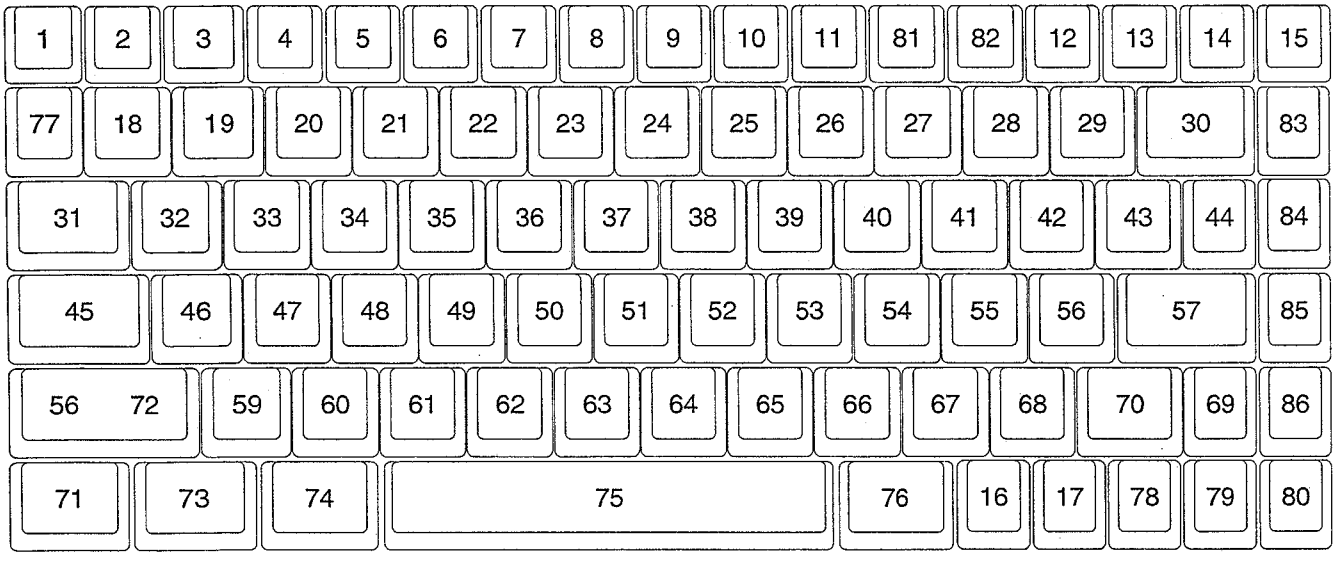


Fig. 4-15: Key Position Number

(2) Keyboard Layout (US)

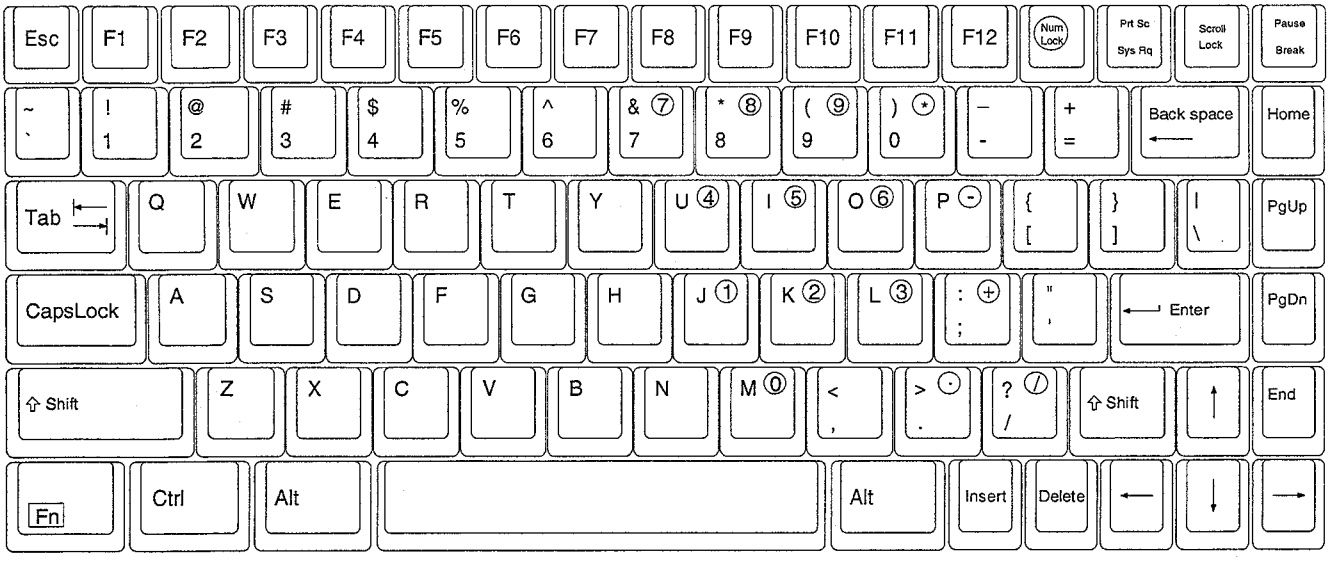


Fig. 4-16: Keyboard Layout (US Engliah)

(3) Keyboard Matrix

CON7

1	S0			49	35	22	62	60	6
2	S1			50	36		63		7
3	S2		5	48	34	21	61	59	
4	S3	4		47	33	20		58	86
5	S4	3		46	32	19	73		
6	S5	2	74	45		18			
7	S6		72	51	37	23		85	8
8	S7	1	75		31	83	71	64	
9	S8		80	57	44	30	70	17	16
10	S9					84	69	79	15
11	S10				43	29	66	78	14
12	S11			56	42	28	67	77	13
13	S12			52	38	24	65		9
14	S13			53	39	27		76	12
15	S14			55	41	26	68	82	11
16	S15		87	54	40	25		81	10
		R0	R1	R2	R3	R4	R5	R6	R7

1 2 3 4 5 6 7 8 CON10

Fig. 4-17: Keyboard Matrix

1. Pin Diagram

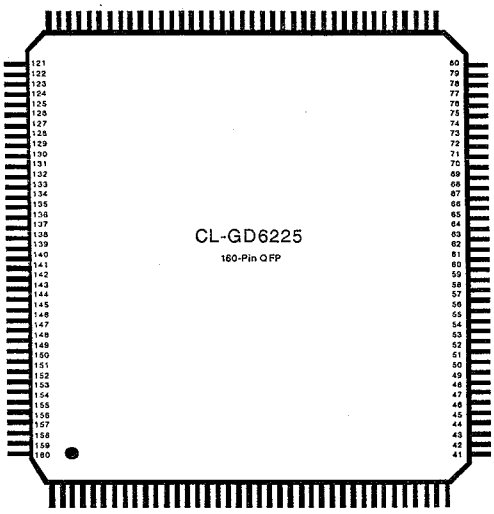


Fig. 4-18: CL-GD6225 Pin Diagram

12. CL-GD6225 VGA

12-1. Overview

The CL-GD62XX (CL-GD6205, CL-GD6215, and CL-GD6225) is a family of advanced single-chip flat panel VGA controllers for use in portable systems with stringent power consumption and form factor requirements. Product family pin compatibility provides easy upgrade capability to color or higher-performance systems.

Integration of the frequency synthesizer, RAMDAC, and monochrome and color STN/TFT panel interface minimizes the form factor requirement for color and monochrome graphics subsystems. All necessarypanel power sequencing logic has been integrated into the CL-GD62XX family, enabling a complete graphics subsystem to be built using only two active components-in less than three square inches. The CL-GD62XX family supports one 256K x 16 DRAM (or four 256K x 4 DRAMs). Additionally, dual-CAS* and WE*-DRAM Configurations are also supported for added flexibility.

The CL-GD62XX family also features SimulSCAN, a technique introduced by Cirrus Logic for achieving simultaneous CRT and LCD operation. It allows portable computers to become a key part of presentation environments for sales-force automation, field service, and educational organizations. SimulSCAN supports both single-and dual-scan LCD panels, and fixed-and multi-frequency analog CRTs.

Proprietary algorithms in the CL-GD62XX family expand the available palette depth for color flat panels. High clock rates provide extended-resolution capability in CRT Mode. At 1024 x 768 resolution, 16 simultaneous colors can be displayed. In 640 x 480 resolution, up to 256 simultaneous colors are available.

12-2. Pin Description

Name	Type	Description
Host Interface --ISA Bus Mode		
AEN	I	ADDRESS ENABLE: If this input is high, it indicates that the ourrent cycle is a DMA cycle. In this case, the CL-GD62XX will not respond to I/O cycles. There is no effect on memory cycle.
BALE	I	BUS ADDRESS LATCH ENABLE: This active-HIGH input is used to latch LA[23:17] on the HIGH-to-LOW transition.
$\overline{\text{BUSCONF}}$	I	BUSCONF: This pin is used in conjunction with $\overline{\text{REF}}$ (LBT0) and $\overline{\text{SMEMW}}$ (LBT1) to establish gthe type of bus the CL-GD62XX is connected to. The '386SL (PI Bus) and Local Bus is supported only in the CL-GD612 5/CL-GD6225.the available configuration.
IOCHRDY	TS	I/O CHANNEL READY: This output, when driven LOW, indicates that additional wait states are to be in serted into the current Display Memory read or write cycle. This output is never driven LOW during I/O cycles or BIOS reads. During a Display Memory read cycle, this signal is always driven LOW as soon as SMEMR* goes active.When the data is ready to be placed on the System Data Bus, this signal is driven HIGH. It remains high until $\overline{\text{SMEMR}}$ goes inactive; it then goes high impedance. During a Display Memory write cycle, if there is space in the Write Buffer, this signal is driven HIGH as soon as $\overline{\text{SMEMW}}$ goes active. If the Write Buffer is full, this signal is driven LOW as soon as SMEMW* goes active and remains LOW until there is space. Once there is space in the Write Buffer, this signal is driven HIGH. It will remain high until $\overline{\text{SMEMW}}$ goes inactive; it then goes high impedance.
$\overline{\text{IOCS16}}$	OC	I/O CHIP SELECT 16: This open-collector output is deiven LOW to indicate that the CL-GD62XX can execute an I/O operation at the address currently on the bus in 16-bit Mode. This signal is generatedfrom a decode of A[15:0] and AEN. table 2-2 indicates the range of addresses for which the CL-GD62XX will generate IOCS16*

Table 2-2. IOCS16* Addresses

Address	Function
3C4, 3C5	Sequencer
3CE, 3CF	Graphics Controller
3B4/3D4, 3B5/3D5	CRT Controller
3BA/3DA	Input Status Register 1

Name	Type	Description
$\overline{IORD}$	I	$\overline{I/O\ READ}$: This active-LOW input is used to indicate that an I/O read is occurring. If the address on SA[15:0] is within the range of the CL-GD62XX, it will respond by placing the contents of the appropriate register on the System Data Bus.
$\overline{IOWR}$	I	$\overline{I/O\ WRITE}$: This active-LOW input is used to indicate that an I/O write is occurring. If the address on SA[15:0] is within the range of the CL-GD62XX, it will respond by transferring the contents of the System Data Bus into the appropriate register. The transfer will occur on the trailing (rising) edge of this signal. A list of I/O addresses to which the CL-GD62XX will respond appears in the description of $\overline{IOCS16}$. When a 16-bit I/O write is done, theaddress specified is typically the Index Register for one of the VGA groups. The index should appear on SD[7:0] and the data should appearon SD[15:8].
IRQ	TS	INTERRUPT REQUEST: This pin is typically unused in PC/AT add-in cards, but may be connected to IRQ2/IRQ9 via a jumper block. See Register CR11 for a description of the controls for this pin.
LA[23:17]	I	ADDRESS [23:17]: These inputs, in conjunction with SA[16:0], are used to select the resource to be accessed during memory.
Host Interface --ISA Bus Mode (cont.)		
$\overline{MEMCS16}$	OC	$\overline{MEMORY\ CHIP\ SELECT\ 16}$: This open-collector output is driven LOW to indicate that the CL-GD62XX can execute a memory operation at the address currently on the bus in 16-bit Mode.
REF*	I	REFRESH: This active-LOW signal indicates that a DRAM refresh is occurring. The CL-GD62XX delays memory read operations occurring when $\overline{REFRESH}$ is active, since it explicitly controls the refresh of Display Memory.
RESET	I	RESET: This active-HIGH signal is used to initialize the CL-GD62XX to a known state, and forces all outputs to three-state.
SA[16:0]	I	ADDRESS [16:0]: These inputs, in conjunction with LA[23:17], are used to select the resource to be accessed during any memory or I/O operation. These address bits must remain valid throughout the cycle.
$\overline{SBHE}$	I	$\overline{SYSTEM\ BYTE\ HIGH\ ENABLE}$: This input is used in conjunction with SA[0] to determine the width and alignment of a data transfer.$\overline{SBHE}$ and SA[0] are decoded as shown inTable 2-4

Table 2-4. SBHE/SA0 Decoding

SBHE*	SA0	Function
0	0	16-bit Transfer
0	1	Upper-byte Transter
1	0	Lower-byte Transfer

SD[7:0]	TS	SYSTEM DATA [7:0]: These bi-directional pins are used to transfer data during any memory or I/O operation. These pins may be connected directly to the corresponding ISA Bus Pins.
SD[15:8]	TS	SYSTEM DATA [15:8]: These bi-directional pins are used to transfer data during 16-bit memory or I/O operations. These pins may be connected directly to the corresponding ISA Bus pins. These pads have pull-up resistors to guarantee a valid input level when not connected.
$\overline{SMEMR}$	I	$\overline{MEMORY\ READ}$: This acvive-LOW input is used to indicate that a memory read is occurring. The CL-GD62XX decodes A[23:15] to determine if a BIOS read is occurring. If so, the CL-GD62XX makes $\overline{EROM}$ active for the duration of $\overline{MEMR}$.
$\overline{SMEMW}$	I	MEMORY WRITE: This acvive -LOW input is used to indicate that a memory write is occurring. The data is latched in the CL-GD62XX on the rising ecdge of this signal, and are actually Transferred to Display Memory later.
2.2 Host Interface --'386SL (PI Bus Mode) *(CL-GD6215/'25 only)*		
$\overline{BUSCONF}$	I	$\overline{BUSCONF}$: This pin is used in conjunction with $\overline{REF}$ (LBT0) and $\overline{MEMW}$ (LBT1) to establish the type of bus the CL-GD62XX is connected to. The '386SL (PI Bus) and Local Bus is supported only in the CL-GD6215/'25.The following table lists the available configuration:

Table 2-5. Bus Type Configuration

Bus Interface	BUSCONF*	LBT0 (REF*)	LBT1 (SMEMW*)
ISA Bus	1	Tie to ISA Bus REFRESH*	Tie to ISA Bus SMEMW*
PI Bus	0	0	0
'386SXL	0	1	0
'386DXL	0	0	1
'486SX/DX	0	1	1

D[15:0]	TS	DATA [15:0]: These bi-directional pins are used to transfer data during memory or I/O operation.
LA[23:17]	I	ADDRESS [23:17]: The PI Bus shares these local address signals with the ISA Bus. These signals provide a path between the '386SL CPU, and the VGA subsystem.
$\overline{PCMD}$	I	$\overline{PCMD}$: This signal indicates that a valid PI Bus cycle is in progress. It can be used as an output enable during PI Bus read cycles. During a PI Bus write cycle, the rising edge of this signal can be used to latch the data on the bus.
$\overline{PM/IO}$	I	$\overline{PM/IO}$: This signal, along with $\overline{PW/R}$, indicates the type of access currently being executed. A memory cycleis indicated by $\overline{PM/IO}$ High, while an I/O cycle is indicated by $\overline{PM/IO}$ Low. $\overline{PM/IO}$ is valid during $\overline{PSTART}$ for PI Bus transfers.
$\overline{PRDY}$	I	$\overline{PRDY}$: This signal terminates a bus cycle. The PI Bus is normally not ready, and a bus cycle will continue until $\overline{PRDY}$ is asserted. $\overline{PRDY}$ must be asserted until the rising edge of $\overline{PCMD}$ to guarantee cycle termination.
$\overline{PSTART}$	I	$\overline{PSTART}$: This input indicates the start of the PI Bus cycle and is used to latch address and status inputs on the HIGH-to-LOW transition.
$\overline{PW/R}$	I	PW/P: This signal, along with $\overline{PM/IO}$, indicates the type of access currently being exected. A write access is indicated by $\overline{PW/R}$ High, while a read access is indicated by $\overline{PW/R}$ Low. $\overline{PW/R}$ is valid during $\overline{PSTART}$ for PI Bus transfers.
SA[16:0]	I	ADDRESS [16:0]: This PI Bus shares these address lines with the ISA Bus. These signals provide extended addressing on the PI Bus and are 86SL CPU outputs during PI Bus cycles.
$\overline{SBHE}$	I	$\overline{SYSTEM\ BYTE\ HIGH\ ENABLE}$: This input is used in conjunction with SA[0] to determine the width and alignament of a data transfer. This signal is latched with $\overline{PCMD}$ Low.

Table 2-6. SBHE#/SA0 Decoding

SBHE	SA0	Function
0	0	16 bit Transfer
0	1	Upper-byte Transfer
1	0	Lower-byte Transfer

$\overline{VGACS}$	I	$\overline{VGACS}$: This signal is asserted when an access occurs to a userdefined VGA memory address space. Accesses to VGA memory transferring across the ISA Bus will also assert this signal. This signal is not asserted during VGA I/O accesses.
Host Interface -- Local Bus (CL-GD6215/'25 only)		
A[23:2]	I	ADDRESS [23:2]: These inputs are used to select the resource to be accessed during memory or I/O operations. A[23:2] are burst address bits for the 486
$\overline{ADS}$	I	ADDRESS STROBE: This active-LOW input indicates that a new cycle has begun. It must be connected directly to the ADS Pin on the CPU.

Name	Type	Description
BE[3:0]	I	BYTE ENABLE [3:0]: These active-LOW inputs are connected directly to the 486DX/'486 Byte Enable Outputs. In the case of the '386SX, BE0 is unused and may be left unconnected. BE1, 2, and 3 are redefined as BHE, BLE, and A1, respectively. They must be connected directly to the corresponding '386 outputs.
BLAST	I	BURST LAST: This pin is used in a 486 system to determine when the end of a burst cycle occurs. It must be connected to the BLAST Pin of the CPU. It is unused in a 486 system and may be unconnected.
BRDY	I	BURST READY: This signal is defined for the 486 only. It is redefined as READY for the '386. It must be connected to the BRDY Pin of the 486. It is used as an output to terminate a CL-GD6215/'25 cycle.
BS16	OC	BUS SIZE 16: This active-LOW output is driven by the CL-GD6215/'25 to indicate that the current cycle addresses a 16-bit resource. The '386DX/'486 will convert the cycle to an appropriate number of 16-bit transfers. This pin is not used for a '386SX Local Bus and may be left unconnected.
CLK1X	I	CLOCK 1X: This is the timing reference for the CL-GD6215/'25 when connected to a '486 Local Bus.It must be connected directly to the corresponding output pin of the CPU. This pin would not be connected in a '386 environment.
RESET	I	CPU RESET: When this active-HIGH input is active, the CL-GD6215/'25 is forced into aninitial condition. It is used to synchronize the CL-GD6215/'25 to CLK2X. This pin must be connected to the RESET Pin of the CPU in a '386 system.
D[15:0]	TS	DATA [15:0]: These bi-directional pins are used to transfer data during any memory or I/O operation. These pins are directly connected to D[15:0] of the '386SX or '386DX Bus. These pins are connected via four bi-directional data transceivers to the 32-bit '486 Data Bus. The transceivers are controlled with OEH, and W/R.
INTR	TS	INTERRUPT REQUEST: This active-HIGH output indicates the CL-GD6215/'25 has reached the end of an active field. Spectifically, the transition occurs at the beginning of the bottom border. See Register CR11 for a description of the controls for this pin.
LBA	OC	LOCAL BUS ACCESS: This open-collector output is driven LOW to indicate that the CL-GD6215/CL-gd6225 will respond to the current cycle. This signal is generated from a decode of A[23:2] and M/IO.This output will be active before the middle of the first timing T2 after an active ADS. This pin is also known as LDEV (VESA Convention).
M/IO	I	MEMORY/IO: This input indicates whether a memory or I/O operation is to occur. It must be connected directly to the M/IO Pin on the CPU.If M/IO is HIGH, a memory operation will occur. If it is LOW, an I/O operation will occur.
OEH	O	OUTPUT ENABLE HIGH: This active-LOW output controls the output enables for the data transceivers that connect the CL-GD6215/'25 SD[15:0] Pins to the '486 D[31:16] Pins.
OEL	O	OUTPUT ENABLE LOW: This active-LOW output controls the output enables for the data transceivers that connect the CL-GD6215/'25 SD[15:0] Pins to the '486 D[15:0] Pins.
READY	TS	READY: This signal is defined for the '386 only. It is redefined as BRDY for the '486. It must be connected directly to the READY Pin of the '386. This active-LOW signal is used as an input to track bus activeity for pipelined cycles. It is used as an output to terminate a CL-GD6215/'25 cycle.
RESET	I	RESET: This active-HIGH input initializes the CL-GD6215/'25 to a known state.
W/R	I	WEITE/READ: This input indicates whether a write or read operation is to occur. It must be connected directly to the W/R Pin on the CPU.If W/R is HIGH, a write will take place. If it is LOW, a read will occur.Dual-Frequency Synthesizer Interface
32KHz	I	32KHz: This input may be selected to source an externally supplied 32KHz clock signal to be used for memory refresh during suspend Mode.
MFILTER	O	MEMORY CLOCK FILTER: This pin must be connected to a PI RC filter returned to AVDD4. The filter components, especially the input capacitor and the resistor, must be placed as close as possible to this pin.
OSC	I	OSCILLATOR INPUT: This TTL input pin supplies the reference frequency for the Dual-frequency Synthesizer. It rrequires an input frequency of 14.31818IS0.01% MHz with a duty cycle of 50IS 10%. This input can be supplied from the appropriate pin on the ISA Bus, or from an oscillator.
VFILTER	O	VIDEO CLOCK FILTER: This pin must be connected to a PI RC filter returned to AVDD1. The filter components, especially the input capacitor and the resistor, must be placed as close as possible to this pin.
Video INterface		
BLUE	O	BLUE VIDEO: This analog output supplies current corresponding to the blue value of the pixel being displayed. See the description of RED for information regarding the termination of this pin.
GREEN	O	GREEN VIDEO: This analog output supplies current corresponding to the green value of the pixel being displayed. See the description of RED for information regarding the termination of this pin.
HSYNC	TS	HORIZONTAL SYNC: This output supplies the horizontal synchronization pulse to the monitor. The polarity of this output is programmable. This pin may be connected directly to the corresponding pin on the feature connector.
IREF	I	DAC CURRENT REFERENCE: The current drawn from AVDD through this pin determines the full-scale output of each DAC. This pin should be connected to a constant-current source.
RED	O	RED VIDEO: This analog output supplies current corresponding to the red value of the pixel being displayed. Each of the three DACs consists of 255 summed current sources. For each pixel, either the 6-bit value from the Lookup Table, or a 5-or 6-bit true-color value is applied to each DAC Input to determine the number of current sources to be summed. Full-scale current on the RED, GReen, and BLUE outputs is related to IREF as follows: *If=(63/30) x IREF* To maintain IBM VGA-output is typically terminated to monitor ground with a 150-ohm 2-percent resistor. This resistro, in parallel with the 75-ohm resistor in the monitor, will yield a 50-ohm impedance to ground. For a full-scale voltage of 700 mV, full-scale current output should be 14 mA.
VSYNC	TS	VERTICAL SYNC: This output supplies the vertical synchronization pulse to the monitor. The polarity of this output is programmable. This pin may be connected directly to the corresponding pin on the feature connector.
Display Memory Intertace		
CAS	O	COLUMN ADDRESS STROBE*: This active-LOW output is used to latch the column address from MA[9:0] into the DRAMs. This pin must be connected to the CAS Pins of all the DRAMs in the Display Memory array.
MA[9:0]	O	MEMORY ADDRESS [9:0]: These pins control the address inputs of the DRAMs. These pins must be connected to the address pins of the DRAMs. MA[9] is used for asymmetric DRAMs only.
MD[15:0]	3S	MEMORY DATA [15:0]:These pins areused to transfer data between the CL-GD62XX and the Display Memory. These pins must be connected to the data pins of the DRAMs.

Name	Type	Description
$\overline{OE}$	O	$\overline{OUTPUT\ ENABLE}$: This active-LOW output is used to control the output enables of the DRAMs. For 256K x 4 DRAMs and 256K x 16 DRAMs with Dual-write Enables, this pin connected to the $\overline{OE}$ Pins of all theDRAMs in the Display Memory array.
$\overline{RAS}$	O	$\overline{ROW\ ADDRESS\ STROBE}$: This active-LOW output is used to latch the row address from MA[9:0] into the DRAMs. This pin must be connected to the $\overline{RAS}$ Pins of all the DRAMs in the Display Memory array.
$\overline{WE[1:0]}$	O	$\overline{WRITE\ ENABLE\ [1:0]}$: These active-LOW outputs are used to control the Write Enable inputs of the DRAMs.
Miscellaneous Pins		
DUALCAS	I	DUALCAS: This input is used to select between a dual-CAS-type DRAM and a dual-WE-type DRAM. If this pin is set to low, then Pin 114 and Pin 126 are defined as $\overline{WE1}$and $\overline{WE0}$, and Pin 127 is $\overline{CAS}$. If this pin is set to high, then $\overline{WE\ [1:0]}$ become $\overline{CAS[1:0]}$, and $\overline{CAS}$ becomes WE.
EROM	O	$\overline{ENABLE\ ROM\ BUFFERS}$: This active-LOW output is used to control the OutputEnable Pins of up to two 8-bit bus drivers. These buffers are used to conncet the data pins of the BIOS EPROMsto the System Data Bus. This output is forced HIGH when RESET is active. This output goes active only for memory read cycles to the Address Range C000:0 through C7FF:F. It is gated with SMEMR* in ISA Mode. It is an unlatched address decode in Local Bus Modes.
INTCLK	I	$\overline{INTCLK}$: This input may be set high at RESET, so that externally supplied clocks can be used for testing. This pin should normally be connected to ground for internal VCO operation.
SW1	I/O	SWITCH INPUT 1: This pin can be used for general input and can be read under register control.
SW2	I	SWITCH INPUT 2: This pin can be used for general input and can be read under register control. NOTE: This pin is readfined as $\overline{BLAST}$ for the '486 Local Bus (CL-GD6215/'25 only).
SW3	I/O	SWITCH INPUT 3: This pin can be used for general input and can be read under register control.
TWR		$\overline{TEST\ LATCVH\ LOAD\ ENABLE}$:This pin is intended for factory testing and must be a no-connect for normal operation. It is internally pulled-up.
Power Management Support		
ACTi	I	ACTi: This pin is an optional-activitysense input. Any low-to-high transitions on this input may be used, with register masking, to reset the internal power-down timers. If not used, this input maybe connected to ground.
FPBACK	O	FPBACK: This output is part of the LCD-panel power-down sequencing, and should be connected to the LCD panel backlight enable.
FPVCC	O	FPVCC: This output is part of the LCD-panel power-down sequencing, and should be connected to the LCD-panel logic power enable.
FPVEE	O	FPVEE: This output is part of the LCD-anel power-down sequencing, and should be connected to hte LCD-panel power enable.
$\overline{LCDRSET}$	I	$\overline{LCDRSET}$: This active-low signal is an optional LCD display reset input. Any high-to-low transition on this input will clear both the LCD and CRT Enable Bits in the CL-GD62XX Power Management Register, and set the Enble Power-Down Sequencing Bit in the LCD Panel Interface Register. This will initiate the LCD-panel power-down sequence. This input has an internal pull-up resistor, and if not used, should be left disc onnected.

Name	Type	Description
NPD	I	NO POWER DOWN: This input can be used to indicate the presence of AC power. If it is driven high, the internal timers will be stopped an prevented from initiating a panel power-down sequence. When this input returns to a low condition, the timers will resume. This pin has an internal pull-down resistor, and may be left disconnected if not used.
STANDBY	I/O	STANDBY: This input may be used to force the activation of Standby Mode, if driven high. This pin can also be programmed as an output and used to indicate the active status. (The output would be pulled high when the CL-GD62XX is in Standby Mode).
SUSPEND	I	SUSPEND: This input is programmable in polarity and is monitored by an internal timer for de-bounce. It can be used to initiate Suspend Mode orturn off the LCD display. The power-on default is active-high.
LCD Panel Interface		
B[5:0]	O	BLUE BITS [5:0]: These bits contain BLUE color data for TFT color LCD panels. See the Flat Panel Intertace Guide for additional panel-connection information.
DE	O	DE: This pin is used to provide the LCD panel with a shift clock enable for flat panels that require it.
FPVDCLK	O	FPVDCLK: This signal is used to drive the LCD panel shift colck, also designated as CP2 by some panel manufacturers.
G[5:0]	O	GREEN BITS [5:0]: These bits contain GREEN color data for TFT color LCD panels. See the Flat Panel Interface Guide for additional panel-connection information.
LD[3:0]	O	LOWER DATA [3:0]: The Lower Data Bits [3:0] are typically used with monochrome dual-scan LCD panels to provide four-bit parallel data for the lower portion of the panel.
LFS	O	LCD FRAME START PULSE: This indicates the start of a new frame on flat panels.
LLCLK	O	LLCLK: This Line Clock output is used to drive the LCD-panel line clock, also designated LP or CP1.
MOD	O	MODULATION: This output provides AC inversion. It should be connected to MOD or AC. Some panel manufacturers provide this function in the panel circuitry.
R[5:0]	O	RED BITS [5:0]: These bits contain RED color data for TFT color LCD panels. See the Flat Panel Interface Guide for additional panel-connection information.
SLD[7:0]	O	COLOR STN LOWER DATA [7:0]: The Lower Data Bits [7:0] are for use with color STN LCD panels and are only available on the CL-GD6225.
SUD[7:0]	O	COLOR STN UPPER DATA [7:0]: he Upper Data Bits [7:0] are for use with color STN LCD panels and are only available on the CL-GD6225.
UD[3:0]	O	UPPER DATA [3:0]: The Upper Data Bits [3:0] are typically used with monochrome dual-scan LCD panelsto proallel data for the upper portion of the panel.
Power Pins		
AVDD[1]	Power	ANALOG VDD (VCLK): This pin is used to supply +3.3 or +5 volts to the Video Clock synthesizer of the CL-GD62XX. This pin must be connected to the VCC rail via a 33-ohm resistor and bypassed to AVSS1

Name	Type	Description
AVDD[3:2]	Power	VDD (DAC): These two pins are used to supply +3.3 or +5 volts to the Palette DAC of the CL-GD62XX. Each pin must be connected directlyto the VCC rail. Each pin must be bypassed with a 0.1-#gF capacitor with proper high-frequency characteristics, as close to the pin as possible. If a multilayer board is used, each VDD Pin must be connected to the power plane. Both pins must be connected to the same voltage.
AVDD[4]	Power	ANALOG VDD (MCLK): This pin is used to supply +3.3 or +5 volts tothe Memory Clock Synthesizer of the CL-GD62XX. This pin must be connected to the VCC rail via a 33-ohm resistor and bypassed to AVSS4 with a 10-#gF capacitor.
AVSS[1]	Ground	GROUND (VCLK): This pin is used tosupply ground reference to the Video Clock synthesizer of the CL-GD62XX.This pin must be connected to the GND rail.
AVSS[3:2]	Ground	GROUND (DAV): These two pins are used to supply ground reference to the Palette DAC of the CL-GD62XX. Each pin must be connected to the GND rail.
AVSS[4]	Ground	GROUND (MCLK): this pin is used to supply ground reference to the Memory Clock Synthesizer of the CL-GD62XX. This pin must be connected to the GND rail.
BVDD[2:1]	Power	BUS VDD[2:1]: These two pins are used to supply +3.3 or +5 volts to the bus interface pin group of the CL-GD62XX. Each pin must be connected directly to the VCC rail. Each pin must be bypassed with a 0.1-#gF capacitor with proper high-frequency characteristics, as close to the pin as possible. If a multi-layer board is used, each VDDPin must be connected to the power plane. Both pins must be connected to the same voltage.
DVDD[2:1]	Power	DRAM VDD [2:1]: These two pins are used to supply +3.3 or +5 volts to the internal DRAM interface pin group of the CL-GD62XX. Each pin must be connected directly to the VCC rail. Each pin must be bypassed with a 0.1-#gF capacitor with proper high-frequency characteristics, as close to the pin as possible. If a multi-layer board is used, each VDD Pin must be connected to the power plane. Both pins must be connected to the same voltage.
CVDD[2:1]	Power	CORE VDD [2:1]: These two pins are used to supply +3.3 or +5 volts to the internal core logic of the CL-GD62XX. Each pin must be connected directiv to the VCC rail. Each pin must be bypassed with 0.1-#gF capacitor with proper high-frequency characteristics, as close to the pin as possible. If a multi-layer board is used, each VDD Pin must be connected to the power plane. Both pins must be connected to the same voltage.
PVDD[1]	Power	LCD PANEL VDD: This pin is used tosupply +3.3 or +5 volts to the LCDflat panel interface pin group of the CL-GD62XX. Each pin must be connected directly to the VCC rail. Each pin must be bypassed with a 0.1-#gF capacitor with proper high-frequency characteristics, as close to the pin as possible. If a multi-layer board is used, this VDD Pin must be connected to the power plane.
Vss[11:1]	Ground	GROUND (LOGIC): These 11 pins are used to supply ground reference to the core logic and pin groups of the CL-GD62XX. Each pin must be connected directly to the GND rail. If a multi-layer board is used, each VSS Pin must be connected to the ground plane.

13. LCD Unit and LCD Controller

13-1. Mechanical Specifications

Parameter	Specifications	Unit
Outline dimensions	266.4 (W) !Q182.8 (H)!Q10.0MAX (D)	mm
Effecive viewing Area	195.0 (W) !Q147.0 (H)	mm
Display format	640 (W)X480 (H) full dots	-
Dot size	0.075XRGB (W)X0.275 (H)	mm
Dot spacing	0.025	mm
1 Base color	Normally black 2	-
Wight	Approx.560	g

1 Due to the characteristics of the LCD material, the colors vary with environmental temperature.

2 Negative-type display
Display data "H" : RGB Dots ON: White
Display data "L" : RGB Dots OFF: Black

13-2. Absolute Maximum Ratings

Electrical absolute maximum ratings

Parameter	Symbol	MIN.	MAX.	Unit	Remark
Supply voltage (Logic)	V_{DD}-V_{SS}	0	6.0	V	Ta=25° C
Supply voltage (LCD drive)	V_{EE}-V_{SS}	0	5.0	V	Ta=25° C
Input voltage	V_{IN}	0		V	Ta=25° C

13-3. Environmental Conditions

Table 3

Intem	Tstg		Topr		Remark
	MIN.	MAX.	MIN.	MAX.	
Ambient temperatuer	-25 ° C	+60 É C	0 É C	+40 É C	Note 4
Humidity	Note 1		Note 1		No condensation
Vibration	Note 2		Note 2		3 directions (X/Y/Z)
Shock	Note 3		Note 3		6 directions (!SX!SY!SZ)

Note 1) Ta= 40 °C.....95% RH Max
Ta= 40 °C.....Absolute bumidity shall be less than Ta=40 °C/95% RH.

Note 2)

Frequency	5Hz~23Hz	23Hz~500Hz
Vibration level	-	1.0G
Vibration width	1.0mm	-
Interval	5Hz!c500Hz!c5Hz/26.6min	

2/hours for each direction of X/Y/Z (6 hours as total)

Note 3) Acceleration : 50G
Pulse width : 11ms
3 times for each direction of !SX/!SY/!SZ

Note 4) Care should be taken so that the LCD Unit may not be subjected to the temperature out of this specification.

13-4. Pin Assignment

(1) CNI

Pin No	Symbol	Description	Level
1	YD	Scan start-up signal	"H"
2	LP	Input data latch signal	H-L
3	XCK	Data input clock signal	H-L
4	DISP	Display control signal	H(ON), L(OFF)
5	V_{DD}	Power supply for logic and LCD (+5V)	-
6	V_{SS}	Ground potential	-
7	VEE	Power supply for LCD (+)	-
8 9 10 11 12 13 14 15	DU0 DU1 DU2 DU3 DU4 DU5 DU6 DU7	Display data signal (upper)	H(ON), L(OFF)

CN2

Pin No	Symbol	Description	Level
16	VSS	Ground poteatial	-
17 18 19 20 21 22 23 24	DL0 DU1 DU2 DU3 DU4 DU5 DU6 DU7	Display data signal (lower)	H(ON), L(OFF)
25	VSS	Ground potential	

(2) CCFT

Pin No	Symbol	Description	Level
1	HV	High voltage line (from Inverter)	-
2	HV	High voltage line (from Inverter)	-
3	NC		-
4	NC		-
5	GND	Ground line (from Inverter)	-
6	GND	Ground line (from Inverter)	-

13-5. Electrical characterictics

Ta=25 ° C, VDD=5V° C5%

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage (Logic)	V_{DD}-V_{SS}		4.75	5.0	5.25	V
Supply voltage (LCD drive)	V_{ZZ}-V_{SS}	Note 1) Note 2)	23.0	26.9	32.6	V
Input signal voltage	V_{IN}	"H" level Note 5)	2.0	-	V_{CC}	V
		"L" level Note 5)	0	-	0.8	V
Input leakage current	I_{IL}	"H" level	-	-	1.0	µA
		"L" level	-1.0	-	-	µA
Supply current (Logic)	I_{DD}	Note 3), Note 4)	-	21.9	32.9	mA
Supply current (LCD drive)	I_{ZZ}		-	15.6	24.5	mA
Power consumption	Pd		-	529.2	960.7	mW

Note 1) The viewing angle #c at which the optimum contrast is obtained by adjusting Vee-VSS.

Note 2) Max. and Min. values are specified as the Max. and Mix. voltage within the condition of peraional temperature range (0!c40 ° C), Typ, value are specified as the typical voltage at 25 ° C.

Note 3) Display high frequency pattern.

V_{DD}=5V, V_{EE}-V_{SS} = (26.9V), Frame frequency = 73Hz, Display pattern = 4bit checker

display
pattern 

Note 4) This value is direct current.

Note 5) TTL Level

13-6. Interface timing rating

Item	Symbol	Rating			Unit
		MIN.	TYP.	MAX.	
Frame cycle	TFRM	(10.52)		16.94	ms
YD signal "H" level set up time	THYS	100			ns
"H"level hold time	THYH	100			ns
"L" level set up time	tLYS	100			ns
"H" level hold time	tLYH	40			ns
LP signal "H" level pulse width	tWLPH	200			ns
XCK signal clock cycle	tCK	82			ns
"H" level clock width	tWCKH	30			ns
"L" level clock width	tWCKL	30			ns
Data get up time	tDS	30			ns
hold time	tDH	30			ns
LP !t allowance time from SCK ↓	tLS	200			ns

Item	Symbol	Rating			Unit
XCK ↑allowance time from LP ↓	tLH	200			ns
Input signal rise/fall time	tr, tf			13	ns

13-7. Characteristics of Backlight

The ratings are given on condition that the following conditions are satisfied

1) Rating (Note)

Parameter	Min	Typ	Max	Unit
Brightness	(50)	70	-	cd/m2

2) Measurement circuit :
CXA-MIOL (TDK) (at IL=5mArms)

3) Measurement equipment :
BM-7 (TOPCON Corporation)

4) Measurement conditions

4-1 Measurement circuit voltage:
DC=13.3V, at primary side
4-2 LCD: All digits WHITE, V_{DD}=5V,
V_{ZZ}-V_{SS}=Vmax, DU0~7="H" (WHITE),
DL0~7="H" (WHITE)
4-3 Ambient temperature: 25°C
Measurement shall be executed 30 minutes after turnign on.

5) Used lamp:

Rating (2pc)

Parameter		Max. allowable value
Circuit voltage (VS)	1,200Vrms MIN.	-
Discharging tube current (IL)	5mArms TYP	7mArms*
Power comsumption (P)	5W	-
Discharging tube voltage (VL)	445Vrms TYP	465Vrms
Brightness (B)	24,000cd/m2 TYP/1pcs	-

Within no conductor closed.

*It is recommended that IL be not more than 5mArms so that beat rediation of CCFT backlight may least affect the display quality.

Operating life
The operating life time is 10,000 hours or more at 5mA. (5,000 hours or more at 7 mA.)

(Operating life with CXA-MIOL or equivalent.)

13-8. Optical Characteristics

Ta=25°C V_{DD}=5.0V, V_{ZZ}-V_{SS}=Vmax

Table 8
Following specs are based upon the electrical measuring conditions, on which the contrast of perpendicular direction (θx=θy=0) will be Max.

Parameter		Symbol	Condition		MIN.	TYP.	MAX.	Unit	Remark
Viewing angle range		θx	C0>5.0	θx=0°	(-30)	-	(30)	dgr.	Note I
		θy		θy=0°	(25)	-	(15)	dgr.	
Contrast ratio		CO	θx=θy=0°		(10)	18	-		Note2
Respon se time	Rise		θx=θy=0°		-	(180)	(250)	ms	Note3
	Decay		θx=θy=0°		-	(120)	(150)	ms	
Unit chroma ticity	White	x	θx=θy=0°		-	0.318	-	-	
		y	θx=θy=0°		-	0.364	-	-	

Note 1) the viewing angle range is defined as shown Fig 4-19.
Note 2) Contrast ratio is defined as follows:

$$CO = \frac{\text{Luminance (brightness) all pixels "White" at Vmax}}{\text{Luminance (Brightness) all pixels "dark" at Vmax}}$$

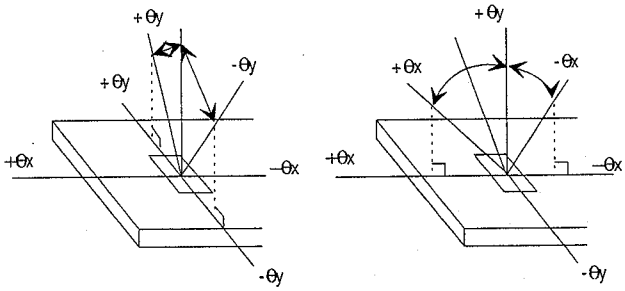


Fig. 4-19: Definition of Viewing Angle

Vmax is defined in Fig. 4-19.
Note 3) The response characteristics of photo-detector output are measured assuming that input signals are applied so as to select and deselect the dots to be measured, in the optical characteristics test method shown in Fig. 4-19.

13-9. Circuit Block Diagram

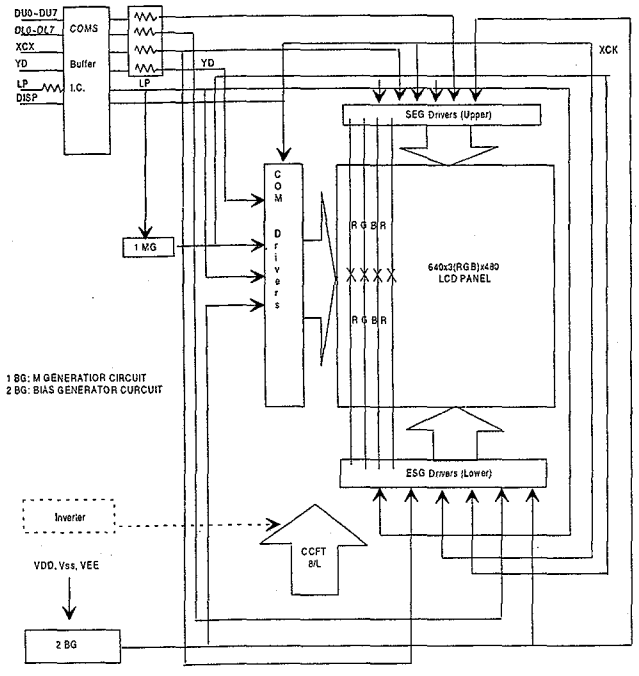


Fig. 4-20: Circuit block diagram

14. Inverter IV18120/T

14-1. Overview

The inverter unit converts the system's low voltage DC supply into a high voltage AC current which can drive the cold cathode fluorescent lamp which illuminates the LCD

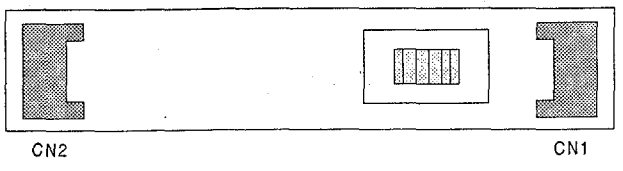


Fig. 4-21: Inverter Unit

screen.

14-2. DC Characteristics

The lamp at max brightness.

	SYMB	MIN	TYP	MAX	UNIT	REMARK
INPUT VOLTAGE	Vin	11	18	24	V	See Test circuit for further detail
INPUT CURRENT	Iin	---	---	330	mA	
LIGHT ON FREQUENCY	F	50	60	70	kHz	
OUTPUT OPEN VOLTAGE	Vs	900	1000	1100	Vrms	
OUTPUT LOAD CURRENT	Iout	5.5	6.0	6.5	mA rms	Rlord 63 Kohm

The lamp at min brightness.

Input Current	Iin	----	----	150	mA	See test circuit for further detail
Light On Frequency	F	50	60	70	kHz	
Output Load Current	Iout	2.5	3.0	3.5	mA rms	Rlord 63 kohm

REMARK: Output load current means that adding a load resistant at output, then meaures the load current.

14-3. Connector Pin Name

14-3-1. CN1 (OUTPUT)

Model No.
M60-04-30-134P

1	HV GND
2	NC
3	NC
4	HV OUTPUT

14-3-2 CN2 (INPUT)

Model No.
M60-04-30-134P

1	VIN
2	CONT (ON/OFF)
3	GND
4	VR

14-3-3. Weight.

Approximation. 9.0 g

14. MK2224FC Hard Disk Drive

14-1. Overview

The MK2224FC comprises a series of intelligent disk drives, hereinafter referred to as the MK2224FC or simply as the drive. The drive features an IBM PC-AT(R) embedded controller that requires a simplified adapter board for interfacing to an AT or AT compatible bus. The drives employ Winchester technology and a closed loop servo control system to realize recording density of more than 190Mbit/inch^2 and average access time of 12 msec with highest reliability of 150,000 hours for MTTF (Mean Time for Failure).
It features as one of the smallest and lightest drives with 19mm height, weighing just 195 grams.
The MK2224FC consists of an HDA (Head Disk Assembly) and a printed circuit board. The HDA is a sealed module and contains a disk spindle assembly, a head actuator assembly and an air filtration system. Reliability is enhanced through the use of Winchester technology. The actuator is a rotary voice coil motor and provides high-speed access.
The disk is driven directly by a DC spindle motor. Air filtration is provided by means of a high performance air filtration system using both breather and circulation filters.
The drive provides a carriage lock mechanism which is activated automatically when power is down, thus preventing head/media damage during non-operating or transportation conditions.
The printed circuit board is located externally to the HDA and contains all the electric circuitries necessary to operate the drive except the head drivers. This board contains the power supply and interface signal connectors. Only the head control IC's are located within the HDA. The circuitries perform the following functions:
Read/Write, Task File Control, Spindle Motor Control, Seek and Head Positioning Servo Control and Abnormal Condition Detection.

14-2. Basic Specification

Capacity (Megabytes)		MK2224FC
Formatted		213
Servo method		Sector Servo on Data Surface
Recording method		1-7 RLL
Recording density		
	TPII	2,840
	BPI	70,500 max
	FRPI	52,900 max
Number of disks		2
Number of data heads		4
Number of user data cylinders		1,560
Bytes per sector		512
Number of sectors per track (User)		
Zone	0	83
	1	79
	2	76
	3	74
	4	69
	5	65
	6	61
	7	57
	8	54
	9	49
Number of cylinders per zone		
Zone	0	156
	1	156
	2	156
	3	156
	4	156
	5	156
	6	156
	7	156
	8	156
	9	156
Number of spare sector per track		1

14-3. Performance

Access time (msec)*1	
Track to track seek *2	3
Average seek *3	12
Max. seek	25
Rotation speed (RPM)	4,000±1%
Average Latency Time (msec)	7.5
Internal Transfer rate (Mbits/sec)	18.9-31.6
Host Transfer rate (Mbytes/sec)	4
Sector Interleave	1:1
Track skew	yes
Buffer size (kBytes)	128
Cache	Read Ahead Cache LRU Segmented
Start time up to Drive Ready	4 sec (TYP.), 20 sec (MAX.)
Stop time (when power switched off)	5 sec (TYP.), 10 sec (MAX.)
Recovery time from Stand-by	4 sec (TYP.)

*1 Under the condition of normal voltage, 25° C normal temperature and of placing bottom side down.

*2 Average time to seek to all possible adjacent track without head switching.

*3 Weighted average time to travel between all possible combination of track calculated as below.

$$\text{weighted average} = \frac{\sum_{n=1}^{Nt} P(n).\ \tau(n)}{\sum_{n=1}^{Nt} P(n)}$$

Nt: Total no. of tracks
P (n): Totel no. of seek for stroke n (=2(Nt-n))
τ (n) : Average seek time for stroke n

*4 Average time for 1,000 full stroke seek with random head switch

14-4. Supply Voltage

14-4-1. Supply for Logic

Allowable voltage range	: 5V +5/-8%
Allowable noise/ripple	: 100mVp-p or less
Current (Typical)	
Starting	: 150mA
Seeking	: 460mA
Reading/Writing	: 450mA
Idle	: 95mA
Stand-by	: 55mA
Sleep	: 15mA

14-4-2. Supply for Motor

Allowable voltage range	: 5V±10%
Allowable noise/ripple	: 109mVp-p or less
Current (Typical)	
Starting	: 450mA
Seeking	: 170mA
Reading/Writing	: 110mA
Idle	: 95mA
Stand-by	: 0mA
Sleep	: 0mA

14-4-3. Power Consumption

	Average(note 3)
Starting	: 3.3W
Reading/Writing	: 3.3W
Seeking	: 3.0W
Idle (note 1)	: 1.0W
Stand-by (note 2)	: 0.3W
Sleep	: 0.12W

(note 1) Motor is rotating in normal speed but none of Reading, Writing or Seeking is executed.
(note 2) Motor is not rotating and heads are parking on CSS (Congtact Start Stop) zone.
(note 3) Under nominal condition(25° C, 1,013mb) and 5V±0%

14-5. Power Sequence

If the 5V Logic is separated from 5V Motor, both lines should be turned on and off within a second longest.

14-6. Dimenson, Weight

Width	: 70.0 mm (2.76")
Height	: 19.0 mm (0.75")
Depth	: 100.0 mm (3.94")
Weight	: 195 g

14-7. Enviromental Limits

14-7-1. Temperature and Humidity

Temperature

Operating	5° C - 55 ° C Gradient 15° C/Hour max
Non-operating	-20° C - 60° C Gradient 15° C/Hour max
Transportation	-40° C - 70° C Gradient 30° C/Hour max

Humidity

Operating	8%R.H - 80%R.H (no condensation)
Non-operating	8%R.H - 80%R.H (no condensation)
Transportation	5%R.H - 90%R.H
Max. wet bulb	29° C

14-7-2. Vibration

Mode	Waveform	Level	Condition
Operating	5-500Hz sine wave sweeping 1 oct./min.	0.5G	no unrecoverable error
Non-operating	5-10Hz 10-500Hz sine wave sweeping 1 oct./min.	25.4mmp-p 5.0G	displacement no unrecoverable error

Shock

Mode	Waveform	Level	Condition
Operating	11msec half sine wave repeating twice max in a minute	10G	no unrecoverable error
Non-operating	11msec half sine wave repeating twice max in a minute	100G	no unrecoverable error
Transportation	Packed in standard box, no unrecoverable error should occur after dropping onto 1 corner, 3 edges or 6 surfaces from 70 cm height		

Altitude

Mode	Waveform	Level	Condition
Operating	-300m to 3,000m		
Non-operating	-400m to 15,000m		

Acoustic Noise

Mode	Waveform	Level	Condition
	Measuring 1.0 meter from the front of drive in normal usage: less than 40dBA		

Safety Standards

Mode	Waveform	Level	Condition
	The MK2224FC disk drives satisfy the following standards: Underwriters Laboratories (UL) 478 and 1950 Canadian Standard ASSOCIATION (CSA) C22.2 No.154 TUV Rheinland IEC 435/VDE 804		

14-8. Reliability

A failure is defined as the inability of the unit to perform its specified function within the requirements of this specification when operated within the defined limits.
Excluded are shipping or handling damage, operator, service or other customer induced failures, adverse environment or failures caused by damaged or faulty systems.

14-8-1. Error Rate

Non-Recoverable Error Rate
1 error per 10^{-13} bits read
The defective sectors allocated to the spare locations in the factory are not included in these error rates.

Seek Error Rate
1 error per 10^{6} seeks
A seek error is a positioning error revoverable with a retry including recalibration.

14-8-2. Mean Time to Failure (MTTF)

The failure means that the drive can not execute the function defined in this specification under the nominal temperature, humidity and other conditions defined in this specification. It should exclude any damage caused by incorrect handling, failure occurred under the condition out of this specification or caused by system failure.

The MTTF is 150,000 hours:

Conditions:

Power on hours:
2,800 hours
(200 days x 14 hours)/year

Operating hours:
1,600 hours
(200 days x 8 hours)/year

Seek hours:
1.30×10^6 seeks/year

No. of start/stop :
5 times/hour (8,000 times/year)

Environment:
Normal (25 °C, 1,013 mb)

14-9. Connector Pin Assignment

The following table describes all of the pins on the Task File Interface.

Signal pin assignment

PIN NO.	SIGNALS	PIN NO.	SIGNALS
1	-HOST RESET	2	GROUND
3	HOST DATA 7	4	HOST DATA 8
5	HOST DATA 6	6	HOST DATA 9
7	HOST DATA 5	8	HOST DATA 10
9	HOST DATA 4	10	HOST DATA 11
11	HOST DATA 3	12	HOST DATA 12
13	HOST DATA 2	14	HOST DATA 13
15	HOST DATA 1	16	HOST DATA 14
17	HOST DATA 0	18	HOST DATA 15
19	GROUND	20	KEY
21	RESERVED	22	GROUND
23	-HOST IOW	24	GROUND
25	-HOST IOR	26	GROUND
27	RESERVED	28	-MASTER/ SLAVE
29	RESERVED	30	GROUND
31	HOST IRQ14	32	-HOST IO16
33	HOST ADDR 1	34	-HOST PDIAG
35	HOST ADDR 0	36	HOST ADDR 2
37	-HOST CS0	38	-HOST CS1
39	-HOST SLV/ACT	40	GROUND
41	+5V (LOGIC)	42	+5V (MOTOR)
43	GROUND	44	RESERVED

Note) Symbol (-) in front of signal name shows negative logic.

14-10. Pin Assignments

SIGNAL NAME	DIR	PIN	DESCRIPTION
$\overline{\text{HOST RESET}}$	$\overline{\text{O}}$ *1)	1	Reset signal from host system; active low during system power-up or detection of voltage fault.
GROUND		2,19 22,24 26,30 40,43	Ground between the drive and the host system.
$\overline{\text{HOST DATA 0-15}}$	I/O	3-18	16 bit bi-directional data bus between the host system and the drive. All 16 bits are used for data transfer in the data register. The lower 8 bits, HD0-HD7, are used for the other register and ECC access.
KEY	N/C	20	An unused pin clipped on the drive and plugged on the cable. Used to guarantee correct orientation of the cable.
$\overline{\text{HOST IOW}}$	O	23	Write strobe, the rising edge of which clocks data from the host data bus, HD0 through HD15, into a register or the data register of the drive.
$\overline{\text{HOST IOR}}$	O	25	Read strobe, low state enables data from a register or the data of the drive onto the host data bus, HD0 through HD15. The rising edge of -HOST IOR latches data from the drive at the host system.
$\overline{\text{MASTER/SLAVE}}$	O	28	Same function as Option Jumper J2 (see 10.7) is provided onto this line. Definition of Master/Slave should be done either by this pin or J2. If J2 is plugged for Master, this line does not affect to the definition. This selection is done by Toshiba Specific command.
$\overline{\text{HOST IRQ14}}$	I	31	Interrupt to the host system, enabled only when the drive is selected and the host activates the -IEN bit in the Digital Output register. When the -IEN bit is inactive high, or the drive is not selected, this output is in a high impedance state, regardless to the state of the interruption. The interrupt is set when the IRQ bit is set by the drive CPU. IRQ is reset to zero when host reads the Status register or a write to the command register.
*1) "I" is from the drive to the host system, "O" is from the host system to the drive, and I/O is bidirectional.			
RESERVED		21,27 28,29 44	Reserved for future use. no connection
$\overline{\text{HOST IO16}}$	I	32	Indication to the host system that the 16 bit data register has been addressed and that the drive is prepared to send or receive a 16 bit data word (open drain).
$\overline{\text{HOST ADDR 1}}$	O	33	Address line from the host system to select the registers of the drive.
$\overline{\text{HOST PDIAG}}$	I/O	34	In Master/Slave mode, reporting the presence of slave drive to master drive and passing diagnostic result between master drive and slave drive.
$\overline{\text{HOST ADDR 0}}$	O	35	Address line from the host system to select the registers of the drive.
$\overline{\text{HOST ADDR 2}}$	O	36	Address line from the host system to select the registers of the drive.

SIGNAL NAME	DIR	PIN	DESCRIPTION
HOST CS0	O	37	Chip select decoded from the host address bus. Used to select one of two groups of host accessible registers.
HOST CS1	O	38	Chip select decoded from the host address bus. Used to select another group of host accessible registers.
HOST SLV/ACT	I	39	Signal from the drive used either: -to drive an external LED whenever the drive is being accessed -or reporting of slave drive's presence to master drive when it is configured as master/slave
+5V (LOGIC)		41	power line for logic and analog circuit
+5V (MOTOR)		42	power line for motor driving

*1) 'I' is from the drive to the host system, "O" is from the host system to the drive, and I/O is bidirectional.

14-11. Host Interface Timing

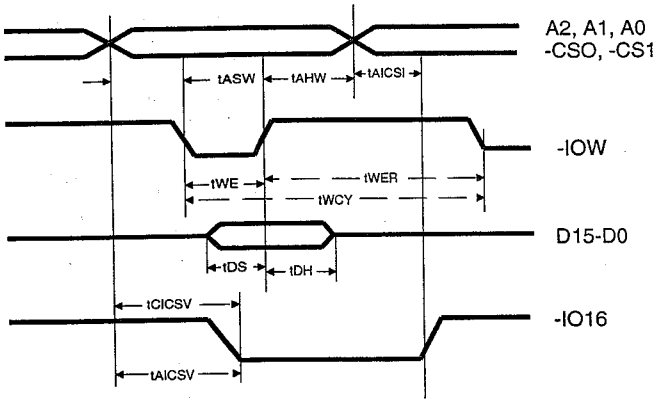


Fig. 4-22: HDD Program I/O Write Timing

Sym	Meaning	Min	Max	Unit	Condition
t_{ASW}	Address Setup to-IOW Low	40		ns	
t_{OS}	Data Setup to -IOW High	50		ns	Data Register
t_{WE}	IOW Pulse Width	75 100		ns	Data Register Other Register
t_{OH}	Data Hold from -IOW High	15		ns	
t_{AHW}	ADDR Hold from -IOW High	20		ns	
t_{WER}	-CS and -IOW Inactive	20		ns	
t_{WCY}	Write Cycle Time	125 150		ns	Data Register Other Register
t_{CICSV}	IO16 valid from -CS		40	ns	
t_{AICSV}	IO16 valid from address		50	ns	
t_{AICSI}	IO16 inactive from address		45	ns	300[50pF Load

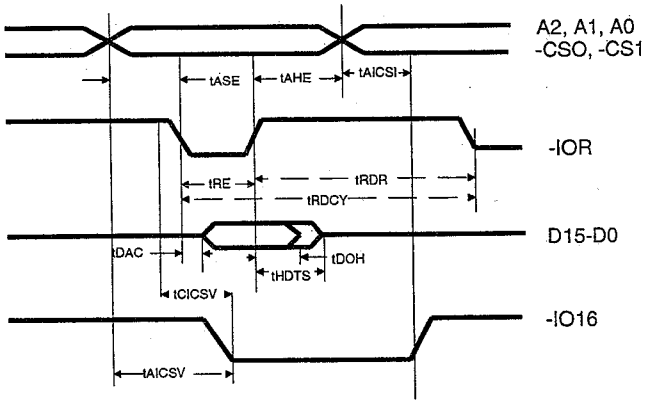


Fig. 4-23: HDD Program I/O Read Timing

Sym	Meaning	Min	Max	Unit	Condition
t_{ASW}	Address Setup to-IOW Low	40		ns	
t_{OS}	Data Setup to -IOW High		60 70 100	ns	Data Register(8 bits transfer) Data Register) Other Register
t_{WE}	IOR Pulse Width	75 100		ns	Data Register Other Register
t_{OH}	Data Hold from -IOW High	5		ns	
t_{AHW}	Data Hold from -IOW High			ns	
t_{WER}	ADDR Hold from-IOR High	10		ns	
	CS and IOW Inactive	20		ns	
t_{WCY}	Read Cycle Time	125 150		ns	Data Register Other Register
t_{CICSV}	IO16 valid from -CS		40	ns	
t_{AICSV}	IO16 valid from address		50	ns	
t_{AICSI}	IO16 inactive from address		45	ns	300Ω50pF Load

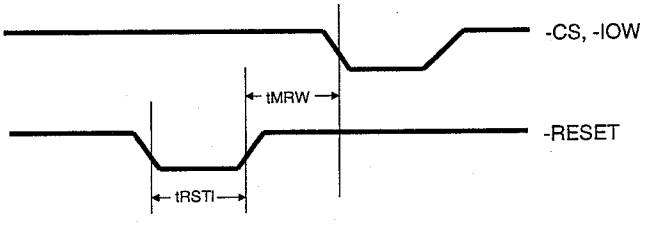


Fig. 4-24: HDD Program I/O Read Timing

Sym	Meaning	Min	Max	Unit	Condition
t_{RSTI}	RESET IN pulse width low	4.0		µs	
t_{MRW}	MR Trailing to host register write	2.4		µs	

14-12 Grounding

HDA (Hard Disk Assembly) and DC ground (ground pins on intertace) are electrically connected to each other.

14-13 Address Decoding

The host addresses the drive using programmed I/O. This method requires that the desired register address is placed on the three host address lines HA2 -HA0, a proper chip select is asserted and a read or write strobe (-HOST LOR/-HOST IOW), is given to the chip.
The following I/O map defines all of the registers.

Address					Read Register	Write Register
-CS0	-CS1	HA2	HA1	HA0		
0	0	X	X	X	Invalid Addr.	Invalid Addr.
0	1	0	0	0	Data Register	Data Register
0	1	0	0	1	Error Register	Write Precomp. Reg.
0	1	0	1	0	Sector Count	Sector Count
0	1	0	1	1	Sector Number	Sector Number
0	1	1	0	0	Cylinder Low	Cylinder Low
0	1	1	0	1	Cylinder High	Cylinder High
0	1	1	1	0	DRVH Register	DRVH Register
0	1	1	1	1	Status Register	Command Register
1	0	0	X	X	High Impedance	Not used
1	0	1	0	X	High Impedance	Not used
1	0	1	1	0	Alt. Status Reg.	Digital Output Reg.
1	0	1	1	1	Digital Input Reg.	Not used
1	1	X	X	X	High Impedance	Not used

The host generates two independent chip selects on the interface. The high order chip select, HOST CS1, is valid only when the host is accessing the three separate register addresses: alternate states
register, digital output register, and digital input register. the low order chip select, HOST CS-, is used to address all other other registers.

14-14. Master/Slave Configuration

By using optional jumper J2 of the interface connector, two units can be connected on a cable in daisy chain. When J2 is open, the drive runs as master drive. In the case of two drives connection, one drive must be set to master and the other drive must be set to slave. If only a single drive is connected to the cable, it must be set to master.
Both master and slave drive are allocated onto the same I/O area and identified the Drive bit in the DRVH register. The host system writes into the register on both drives but reads the register only from a selected drive.
Only the selected drive can exectue the command except for the Diagnose command. The Diagnose command is executed on both drives and the result of the slave drive is transferred to the master drive through the PDIAG line. The master drive reports both results to the system.

HDD Interface Connector

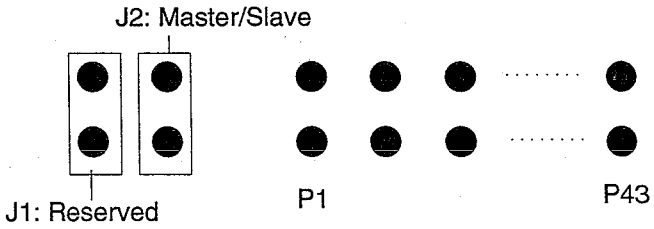


Fig. 4-25: HDD Reset Timing

15. AC Adapter

15-1. Specififcation

Normal Input Voltage	115/230 volts AC
Line Frequency Range	47 Hz to 63 Hz
Operating Voltage Range	90-264 volts AC. The power supply is capable of operating at either voltage.
Input Surge Voltage	400 volts AC for 50ms maximum without damage to the power supply and any changes on the output voltages outside the regular specifications.
Input Connector	CE-22 type IE connector.
Normal Input Current	1.0 A RMS MAX. at 115 volts ac under full output load. 0.5 A RMS MAX. at 230 Volts ac under full output load.
Surge Current	30 A peak at cold start for ½ cycle at any input voltage within regular specifications.
Leakage Current to GND	3.5 mA maximum at 115/230 Vac, 50/60 Hz.
Indicator	Power On: LED 1 Green No Charging : LED 2 Off In Charging: LED 2 Orange Charge Full: LED 2 Off protection Circuit Active: LED 1/LED 2 Flashing

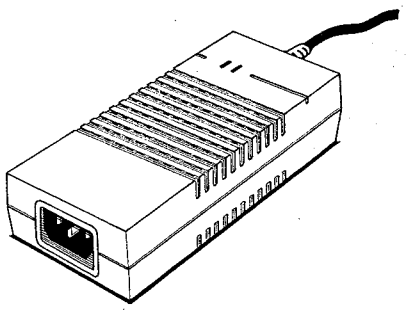


Fig. 4-26: AC Adapter

(1) General Properties

Hold up time	The power supply is capable of riding through min. ½ cycle of AC interrupt at nominal ac, 50/60 Hz frequency, 100% DC output load
Efficiency	65% minimum at nominal continuous input line and full-rated output power.
Overshoot / Undershoot	The power supply exhibits ± 10% overshoot and undershoot of the regulation band at turn on / turn off.
Audible Noise	The unit has no audible noise (0-20 kHz) at any combination of line or load specified. The overall noise does not exceed 45 dB when measured at a distance of 1 meter.
No load conditions	The power supply exhibits no catastrophic failure at a no load condition.
Temperature stability	± 3% for 8 hours following initial 5 minutes warm up.
Returns	All returns are common to chassis ground.
Power on delay time	All output voltages reach regulation specifications within 1 second under any specified input range.
Short circuit	All outputs can withstand a short circuit indefinitely without damage to the power supply.
Reverse voltage protection	No reverse polarity voltage protection is required.
Temperature coefficiency	± 0.03% /°C maximum for all outputs

15-2. Detail Specification

15-2-1. DC Output Power

Output Power	a) +21.2 V/1.0 A and 20.4 V/80mA =22.83 watts b) +21.2 V/0.2 A and 20.4 V/ 1.2A = 28.72 watts
Output Voltage	+21.2 V (+5%, -3%) at the end of the DC output connector
Output Current	0 A minimum to 1.0 A maximum (surge 1.6 A)
Regulation	+5%, -3% for any combination of line, load, cross regulation and centering. Worst case regulation shall be a 0% to 100% load change with all other voltages at nominal load.
Ripple and Noise	200mV p-p at full load 20 kHz to 500 kHz. 100mV p-p for frequencies below 1kHz/100mV p-p noise and spike 500 kHz to 20 MHz
Overvoltage protection (OVP)	Overvoltage protection at 23.0V to 30.0V of the output voltage
Overcurrent Protection (OCP)	Overcurrent protection at 2.0A -3.0A of the output current
Protection	The diode must be added in the output of 21.2 V end of PCB

Charging Current Output

Output Current	1.2 A constant current when battery is not full or the system is turned off. (The current consumption is not more than 0.2 Amps) 20-80mA constant current when battery is full or the system is turned on (the current consumption is more than 0.2 Amps.)
Clamp Voltage	20.4 Volts (+4% /-0%), even 0 amp at 21.2 V
Ripple and Noise	200mV p-p at full load 20kHz to 500kHz. 100mV p-p for frequency below 1kHz and 50mV p-p noise and spike 500kHz to 20MHz.
Protection	The diode must be added in the output of 1.2 A constant current end of PCB.

Charging Method

Delta V	Detects less than 100mV Negative Delta Voltage
Initial Charging	2-4 minutes don't care period
Fast Charging	Constant current 1.2 A charging
Trickle Charging	Constant current 20-80mA charging
Time Protection	Turn off charger when charging is out of time (140-180 minutes)
Thermal Protection	Detects 50°C ± 3°C to cut off fast charge and change to trickle charge
Indicator	Power On: LED1 Green No Charging: LED2 Off In Charging: LED2 Orange Charge Full: LED2 Off Protection: LED1&2 flash

15-3. Environmental

Ambient Operating Temperature	The unit can operate from +4°C to +40°C
Storage Temperature	-40°C to +85°C
Relative Humidity	+10% to +90%, non-condensing with all other maximum "worst case" parameters imposed.

15-3-1. Dimensions

150mm long x 70mm wide x 38mm high
Approx 400g weight

15-3-2. Output Cable Connector

The cable length is 1800mm

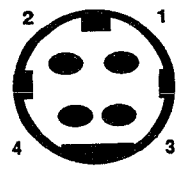


Fig. 4-27: Output Cable Mini-DIN Connector

Pin	Signal	Description	Cable Color
1	+21.2V/1.0A	For motherboard	Red
2	+20.4V/1.2A	For charging	Yellow
3	Thermal detect		White
4	GND	For GND	Black

16. Nickel-Metal Battery

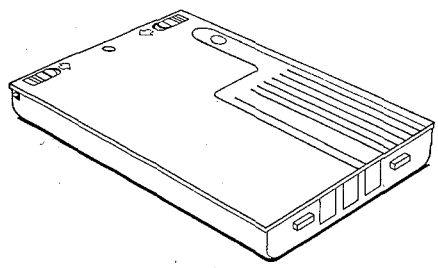


Fig. 4-28: Nickel-Metal Battery

16-1 Specifications

Type	Rechargeable Nickel-Metal hydride
Weight	1.298 pounds (0.59kg)
Nominal Capacity	2300mA
Nominal Voltage	14.4V
Standard Charging Current	230mA
Temperature (recommended)	
Charge	0° C to 45° C
Discharge	-20° C to 60 C
Storage	-30° C to 50° C
Storage (Long Period)	-30° C to 35° C

17. Expansion Connector

Fig. 4-29: Expansion Connector

Connector Pin Assignment

Pin	Signal	Pin	Signal
1	Printer - STROBE	2	Printer - AFD
3	Printer - Data 0	4	Printer - ERROR
5	Printer - Data 1	6	Printer - INIT
7	Printer - Data 2	8	Printer - SLCT IN
9	Printer Data 3	10	Printer Data 4
11	GND	12	GND
13	Printer Data 5	14	Printer Data 6
15	Printer Data 7	16	Printer - ACK
17	Printer BUSY	18	Printer PE
19	Printer SLCT	20	Com 1 carrier detect (RS232)
21	Com 1 Data set ready (RS232)	22	Com 1 Receive Data (RS232)
23	GND	24	GND
25	Com 1 Request to send (RS232)	26	Com 1 Transmit Data (RS232)
27	Com 1 Clear to send (RS232)	28	Com 1 Data Terminal Ready
29	Com 1 ring dectect (RS232)	30	ISA Data 0
31	ISA Data 1	32	ISA Data 2
33	ISA Data 3	34	ISA Data 4
35	GND	36	GND
37	ISA Data 5	38	ISA Data 6
39	ISA Data 7	40	ISA Data 8
41	ISA Data 9	42	ISA Data 10
43	ISA Data 11	44	ISA Data 12
45	ISA Data 13	46	ISA Data 14
47	GND	48	GND
49	ISA Data 15	50	ISA Reset
51	ISA - Refresh	52	ISA - SMEMR
53	ISA - SMEMW	54	ISA - IOR
55	ISA - IOW	56	ISA - MEMR
57	ISA - MEMW	58	GND
59	GND	60	ISA - DACK 7
61	ISA - DACK 6	62	ISA - DACK 5
63	ISA - DACK 3	64	ISA - DACK 2
65	+5V	66	HDD D0
67	+5V	68	ISA - DACK 1
69	+5V	70	HDD D1
71	HDD D2	72	ISA - $\overline{\text{DACK}}$
73	HDD D3	74	HDD D4
75	+5V	76	ISA DRQ 0
77	+5V	78	HDD D5
79	+5V	80	ISA DRQ 1
81	+5V	82	HDD D6
83	HDD D8	84	ISA DRQ 2
85	Battery charge	86	HDD D9
87	Battery charge	88	ISA DRQ 3
89	Battery charge	90	HDD D10
91	HDD D11	92	ISA DRQ 5

Pin	Signal	Pin	Signal
93	POWER 21V	94	HDD D12
95	POWER 21V	96	ISA DRQ 6
97	POWER 21V	98	HDD D13
99	POWER 21V	100	ISA DRQ 7
101	MODEM Line 1	102	MODEM Line 2
103	HDD D14	104	HDD D15
105	Com 2 Data terminal ready (TTL)	106	Com 2 Clear to send (TTL)
107	Com 2 Transmit data (TTL)	108	Com 2 Request to send (TTL)
109	Com 2 Receive data (TTL)	110	Com 2 Data set ready (TTL)
111	Com 2 Carrier detect (TTL)	112	Com 2 RING detect (TTL)
113	Com 2 Disable	114	+5V
115	MOUSE Clock (PS2)	116	MOUSE Data (PS2)
117	Keyboard Data	118	Keyboard Clock
119	HDD - DIAG	120	HDD - ACT
121	HDD - HDCS	122	HDD D7
123	HDD - Reset	124	HDD - CS1
125	HDD - CS Φ	126	GND
127	GND	128	ISA IRQ 3
129	ISA IRQ 4	130	ISA IRQ 5
131	ISA IRQ 6	132	ISA IRQ 7
133	ISA IRQ 9	134	ISA IRQ 10
135	ISA IRQ 11	136	ISA IRQ 12
137	ISA IRQ 14	138	GND
139	GND	140	ISA SYSCLK
141	ISA - IOCHCK	142	ISA - Φ WS
143	ISA - MEMCS16	144	ISA - IOCS16
145	ISA TC	146	ISA BALE
147	ISA - MASTER	148	ISA - SBHE
149	ISA AEN	150	IOCHRDY
151	GND	152	GND
153	ISA address 0	154	ISA address 1
155	ISA address 2	156	ISA address 3
157	ISA address 4	158	ISA address 5
159	ISA address 6	160	ISA address 7
161	ISA address 8	162	ISA address 9
163	GND	164	GND
165	ISA address 10	166	ISA address 11
167	ISA address 12	168	ISA address 13
169	ISA address 14	170	ISA address 15
171	ISA address 16	172	ISA address 17
173	ISA address 18	174	ISA address 19
175	ISA address 20	176	GND
177	GND	178	ISA address 21
179	ISA address 22	180	ISA address 23
181	FDD - INDEX	182	FDD - DS1
183	FDD - DCHG	184	FDD - MD1
185	FDD - DIRC	186	FDD - STEP
187	FDD - Write Data	188	GND
189	GND	190	FDD - TRACK Φ
191	FDD - Write enable	192	FDD - Read Data
193	FDD - Write protect	194	FDD - RWC
195	FDD - Head select	196	CRT Red
197	CRT Green	198	CRT Blue
199	CRT Vsyne	200	CRT Hsync

Jumper & Swich Setting

(1) SW1

Switch \ CPU	486DX/DX2	486SX
SW1	ON	OFF
SW2	ON	OFF
SW3	ON	OFF
SW4	OFF	ON

CPU SPEED

Frequency Switch	25M	33M
SW5	ON	OFF

PANEL TYPE

Switch \ LCD	MONO	TFT	Dual Color STN
SW6	ON	ON	ON
SW7	ON	OFF	OFF
SW8	OFF	OFF	ON

(2)SW2

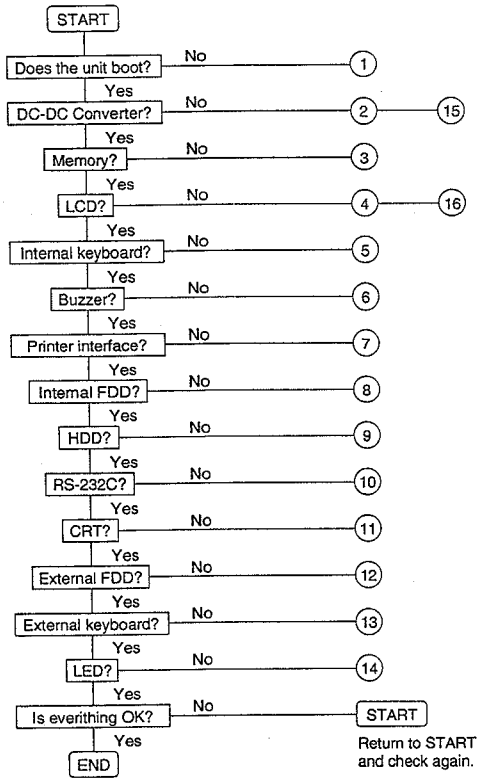
Switch SW2 is a push button switch. Push then release it to turn on power of system. Push again to power off system.

(3) J2

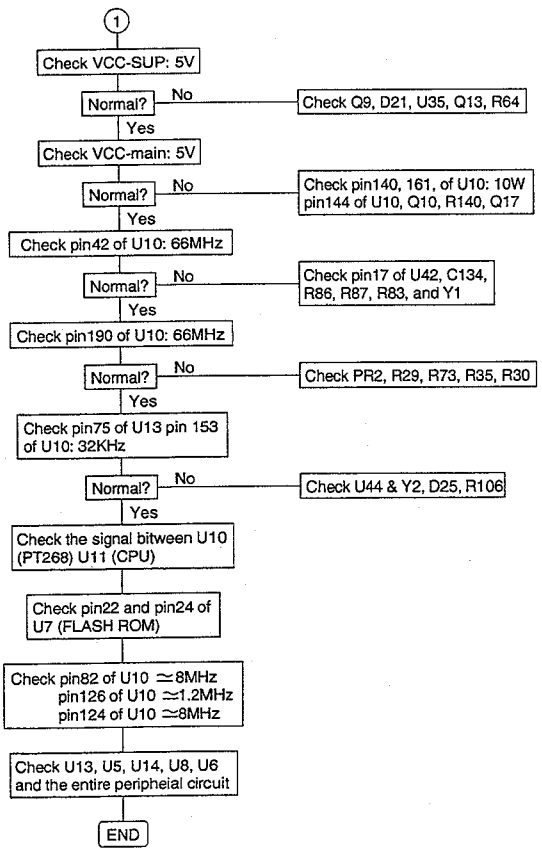
State	Jumper OFF	Jumper ON
J2	Password Enabled	Password Disabled

CHAPTER 5. TROUBLE SHOOTING

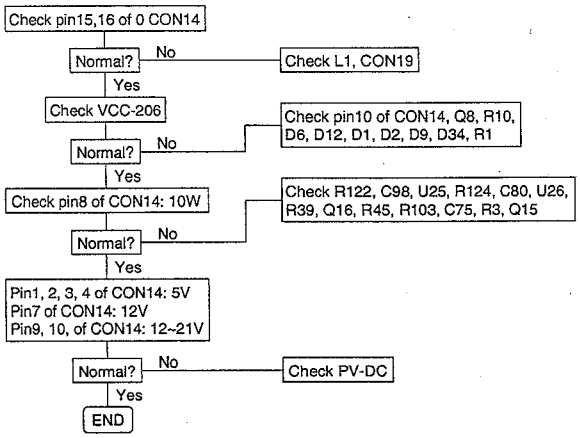
1.General



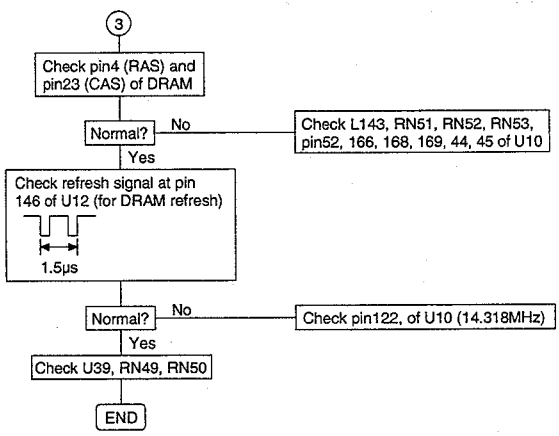
1-1. Will not start



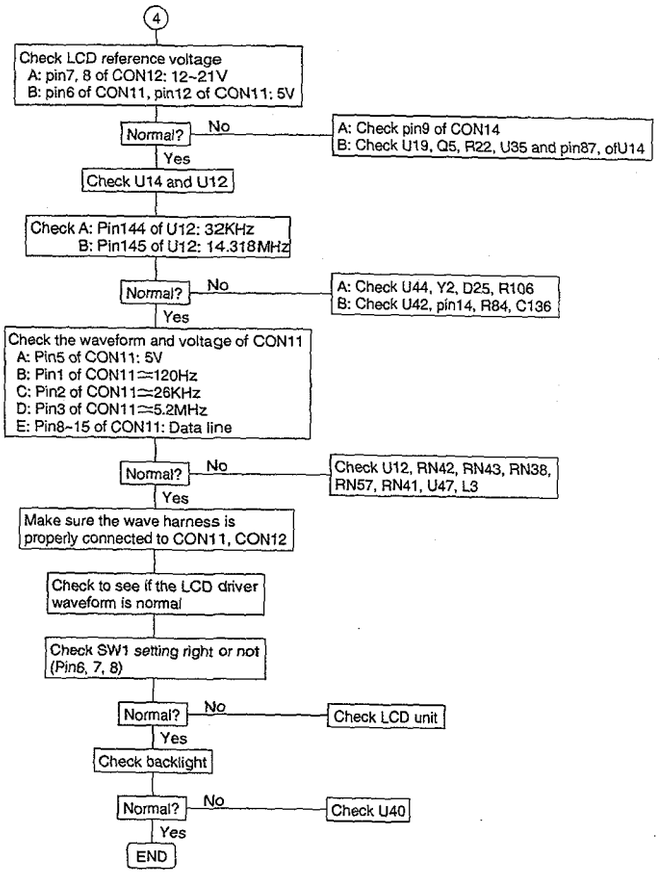
1-2. DC T0 DC converter check



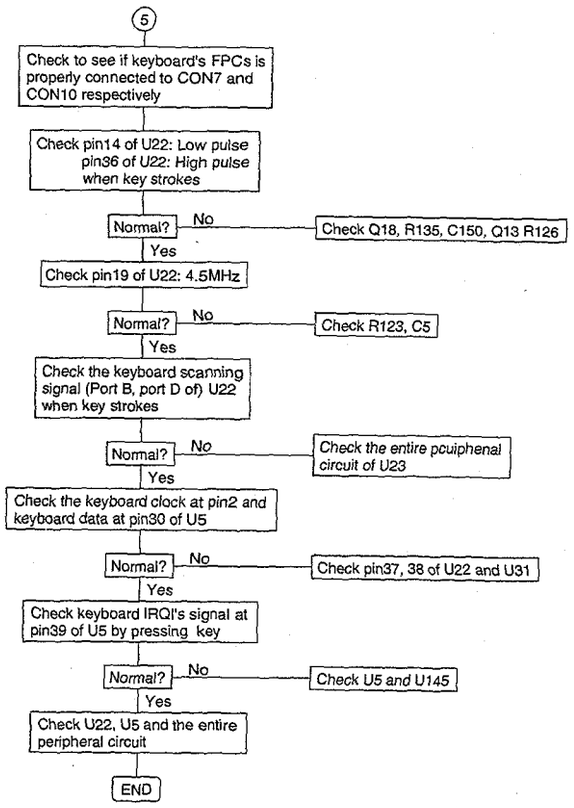
1-3. MEM check



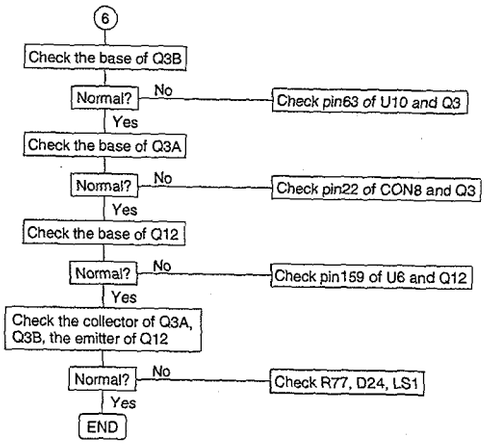
1-4. LCD check



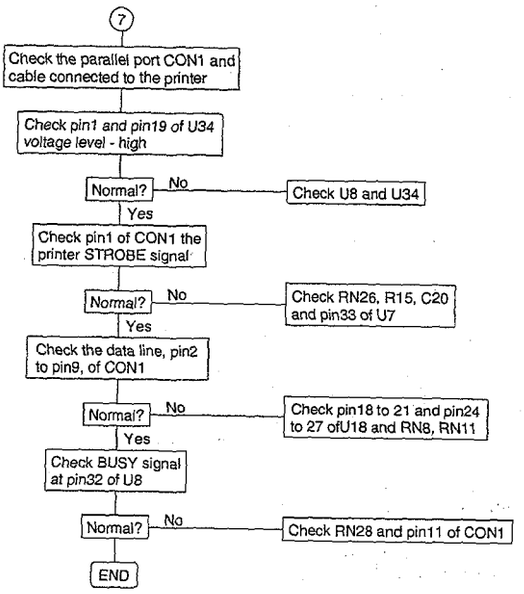
1-5. Internal keyboard check



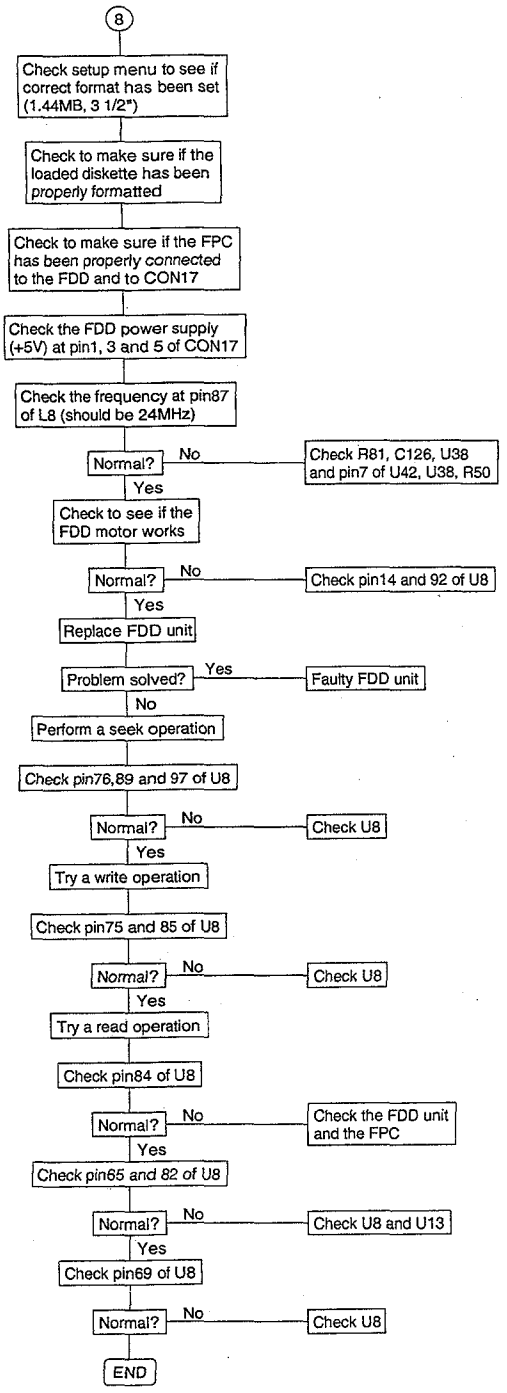
1-6. Buzzer check



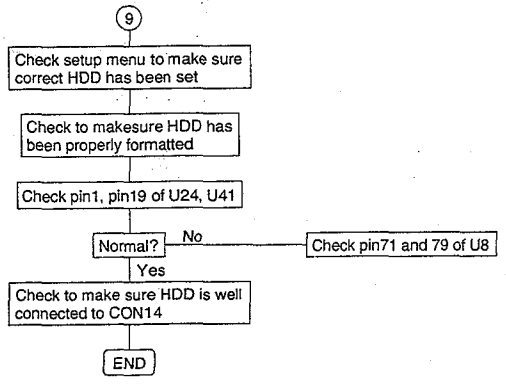
1-7. Printer interface check



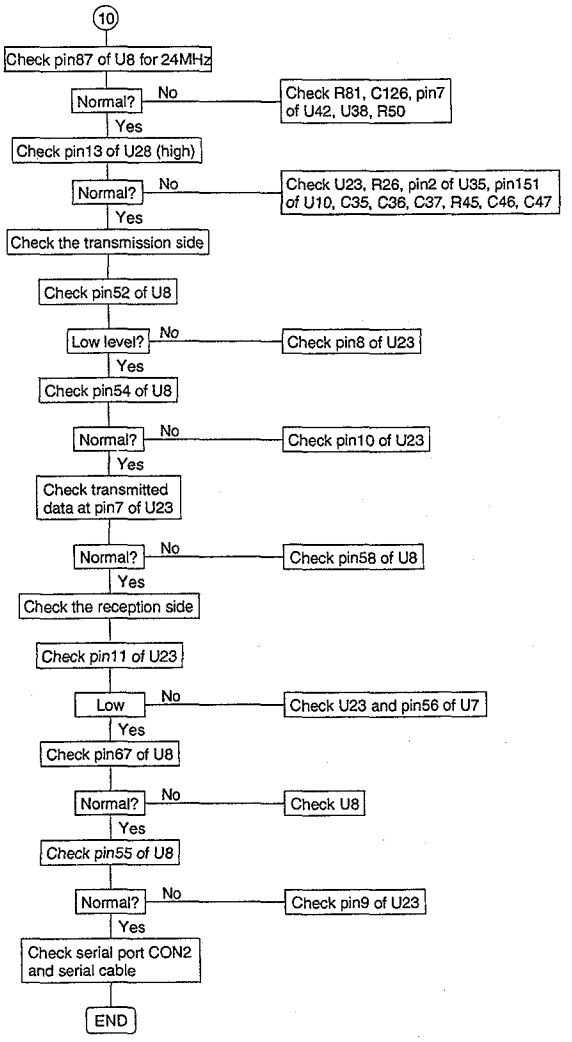
1-8. Internal FDD check



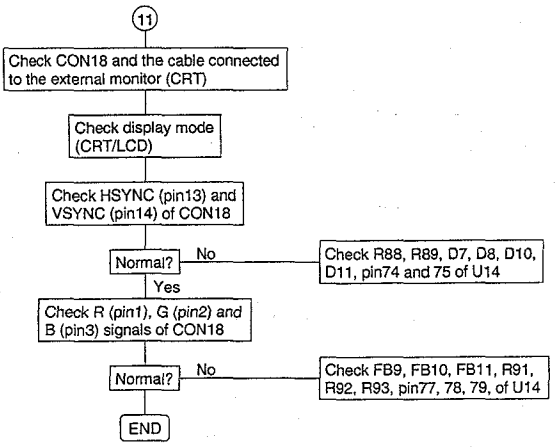
1-9. HDD check



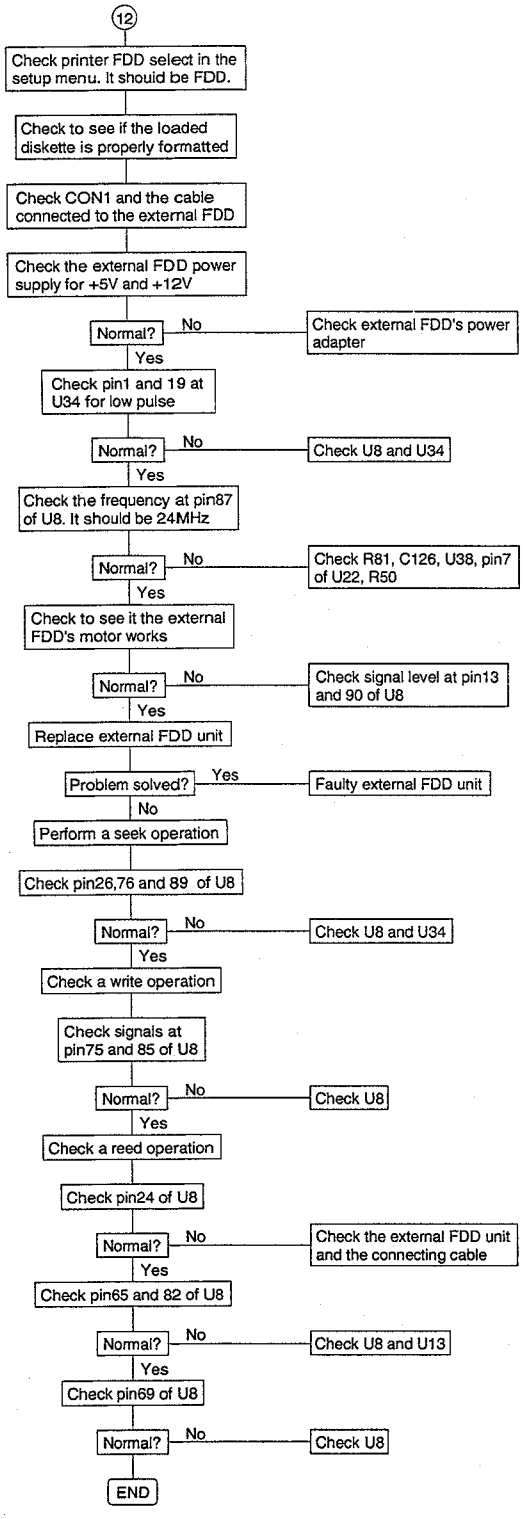
1-10. RS-232C check



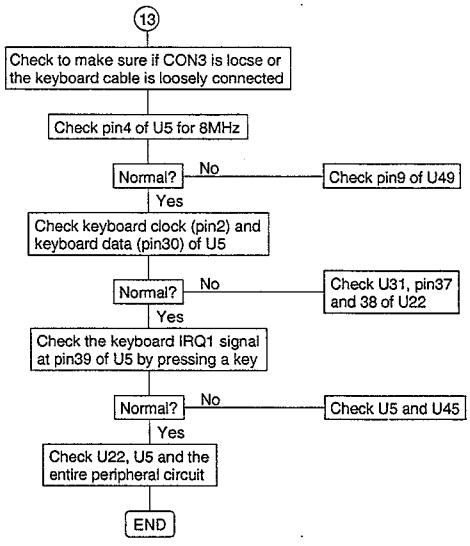
1-11. External CRT check



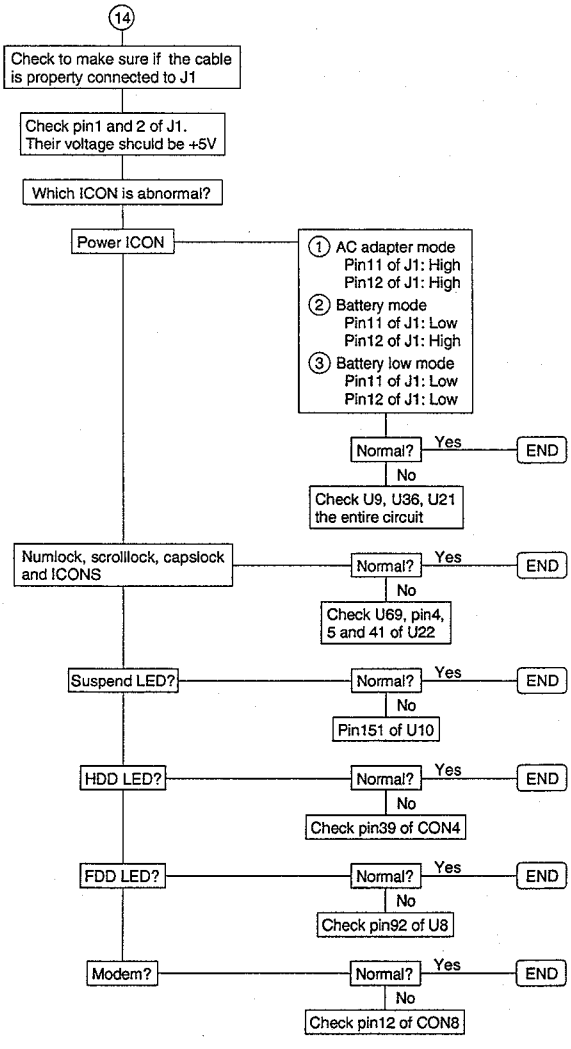
1-12. Check external FDD



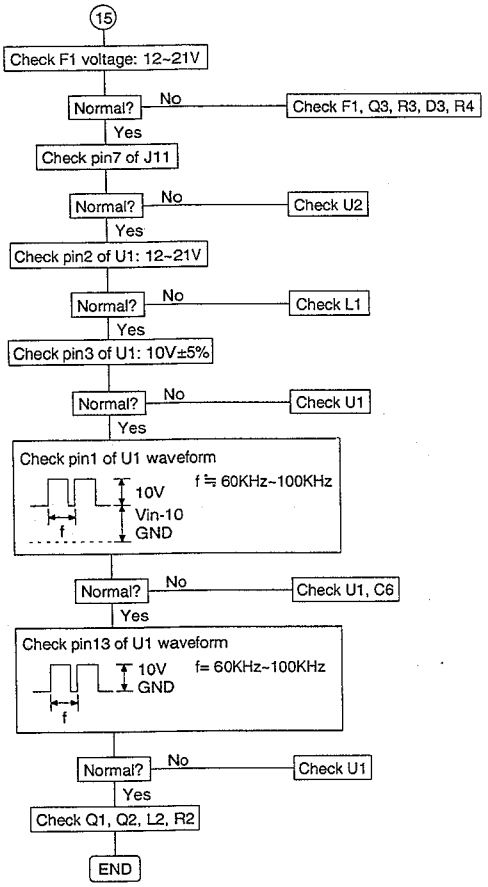
1-13. External keyboard check



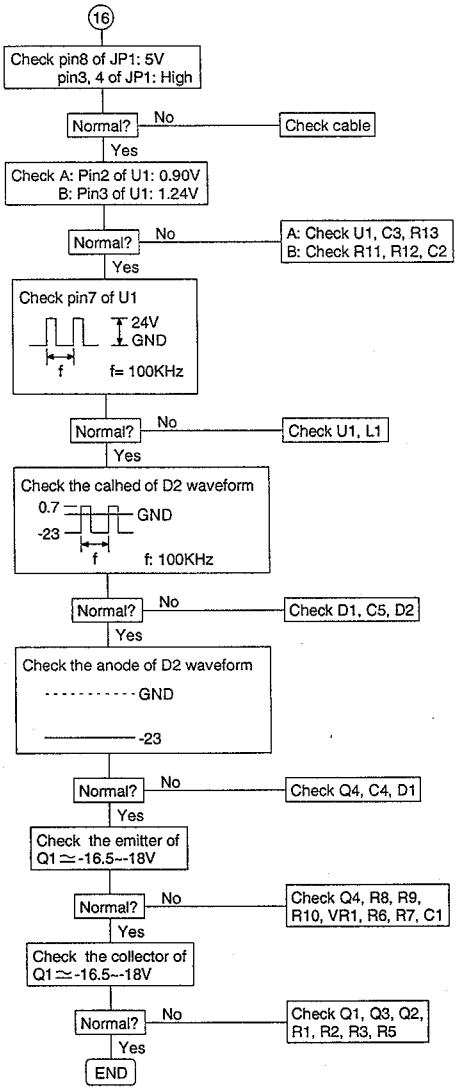
1-14. Check LCD indicator



1-15. PV-DC card



1-16. PV-VRM



CHAPTER 6. DIAGNOSTICS

There are two diagnostic routines available to check that your computer and its peripherals are functioning as they should. One routine is automatic, and takes place every time you turn on the power. The other is accessed from a separate diagnostic program on the Support diskette.

1) Power-On Diagnostics

When the system power is turned on, an automatic self-test routine starts. The routine checks internal memory and displays a count of the number of KB available as it checks.
After a few seconds, MS-DOS starts to load, and the following screen is displayed:

```
Starting MS-DOS...
```

before displaying the MS-DOS start-up message. If MS-DOS fails to load from the hard disk (or a diskette), an error message appears on the screen.
Turn off the power, wait five seconds, then turn it on again. If the error message appears repeatedly.
Refer to the Appendix E, "BIOS Messages", for a list of power-on error messages.

2) Diagnostic Program

If the power-on diagnostic routine doesn't display any messages, but you suspect that there is a problem, run the diagnostic program included on your Support diskette.
The diagnostic program contains the following checks:

- Real Time Clock
- Memory
- Keyboard
- Video Subsystem
- Liquid Crystal Display
- Floppy Disk Drive
- Printer
- Hard Disk Drive

Creating a Backup Copy of the Diagnostic Program

The diagnostic program should always be run from drive A.
Therefore you should make a backup copy from the Support diskette to a new diskette which has been formatted using the /S (system) switch for use as a start-up disk.

At the C:\> prompt, follow these steps:

1. Insert a new diskette into drive A. From the Windows Program Manager, open the File Manager icon.
2. From the Disk menu, choose Format Disk. In the Capacity box, select the size of the Disk you want to format, and select Make System Disk check box, then choose OK to format the new diskette.
3. Select the a drive icon. From the Disk menu, choose Copy Disk. Follow the instruction to make a backup copy of the Support diskette.

You have now created a backup copy diskette. To run the diagnostic program you should always use this backup copy diskette.

Starting the Diagnostic Program

Insert the backup copy diskette into the floppy disk drive, start up the computer, and, at the A:\> prompt, type

```
DIAG
```

and press **Enter**. The diagnostic program starts up. This may take several seconds. The main menu is then displayed on the screen.
Use the cursor keys to move the bar cursor to the particular diagnostic test you want to run and press **Enter**. Or, press **Esc** to exit the diagnostic program and return to the A:\> prompt.
Some of the diagnostic test categories on the menu contain several separate tests. When you select one of these categories, a separate sub-menu is displayed. You can exit the sub-menu and return to the main menu by pressing **Esc**. Each category is described below.

Caution: If you have installed the internal trackball, do not touch it while you are checking your computer with the diagnostics program.

Real Time Clock (RTC)

This category contains the following three tests:

RTC Timer Check

Checks if the timer interrupt works correctly.

RTC Clock Check

Checks if the clock works correctly.

CMOS RAM Check

Does a data read/write check on the special battery backed-up memory area used for the real-time clock.

Run All Checks

Checks all three of the above items in sequence.

Memory

This category contains the following checks:

Caution: These checks will destroy the contents of the memory.

Conventional Memory Check

Reads/writes data in the conventional memory area. The check stops at the first error and displays an error message.

Extended Memory Check

Reads/writes data in the extended memory area. The check stops at the first error and displays an error message.

Run All Checks

Checks both the two items above in sequence.

Keyboard

After selecting this test, you are prompted for the keyboard type.
Move the bar cursor using the cursor keys to select either the U.S. English keyboard or other keyboard types and press **Enter**.
The keyboard test begins with a graphic representation of the keyboard layout displayed on the screen. To test whether a particular key functions properly, press the key. A square should display on the keyboard layout at that position if the key is working correctly.

Video Subsystem

This test checks that the built-in video subsystem is working properly. The video subsystem menu is displayed on the screen with the following categories:

Video Memory Check

Checks the buffer in the video subsystem.

DAC Check

Checks the digital-to-analog converter in the VGA subsystem.

Attribute Check

Displays 16 foreground, 8 background, and 8 blinking shades of gray.

Character Set Check

Displays characters on the screen normally on an 80 × 25 text mode display.

Run All Checks

Runs all four of the above checks in sequence.

Liquid Crystal Display

This test checks the computer's LCD screen. Three test patterns are displayed. A defect in any pattern indicates a faulty screen.

Checker Pattern Check

A checked pattern is displayed.

Stripe Pattern Check

A striped pattern is displayed.

Shade of Color Check

32 shades of color are displayed.

Run All Checks

Runs all three checks in sequence.

Floppy Disk Drive

This test reads and writes data continuously to a diskette in the floppy disk drive to test the read/write functions of the drive. After selecting the test, the floppy drive sub-menu is displayed with the following categories:

Caution: As the write-read check may erase data from the diskette in the drive under test, use a blank diskette or one containing data that you no longer need.

Read Check

Checks that data can be read from the diskette without errors. The test stops if an error is detected and displays an error message.

Write-Read Check

Checks if data can be written/read correctly by comparing data written to the diskette with data read from the diskette. This test destroys all existing data on the diskette. The test stops if an error is detected and displays an error message.

Printer

This test checks the operation of the printer, if one is connected. After selecting the test, the printer sub-menu is displayed on the screen with the following categories:

Status Check

The printer status signals are checked and displayed.
The following status categories are checked:

- **Bsy** checks the printer busy signal
- **Ack** checks that the printer can handshake with the computer
- **Pe** checks that the paper is set
- **Sel** shows when the printer is on-line
- **Ioe** checks that the printer's mechanical components are functioning properly

An asterisk is displayed below a category when its check completes normally.

Print Check

Test printing will not start until the five status categories in the status check all show an asterisk (below the category). If a hardware malfunction is detected, an asterisk will not appear below the corresponding category. In this case, you will not be able to do a test print. Make a note of the error message.
Once all categories contain asterisks, press any key. The system returns to the printer sub-menu. Try the print check. A test pattern should print.

Hard Disk Drive

This test reads and writes data continuously to the hard disk to test the read/write functions of the drive. After selecting the test, the hard disk sub-menu is displayed on the screen.

Caution: DO NOT run the hard disk drive write-read check on the diagnostic progarm unless you have exhausted all other possibilities, because the test will destroy all existing data on your hard disk.

Read Check

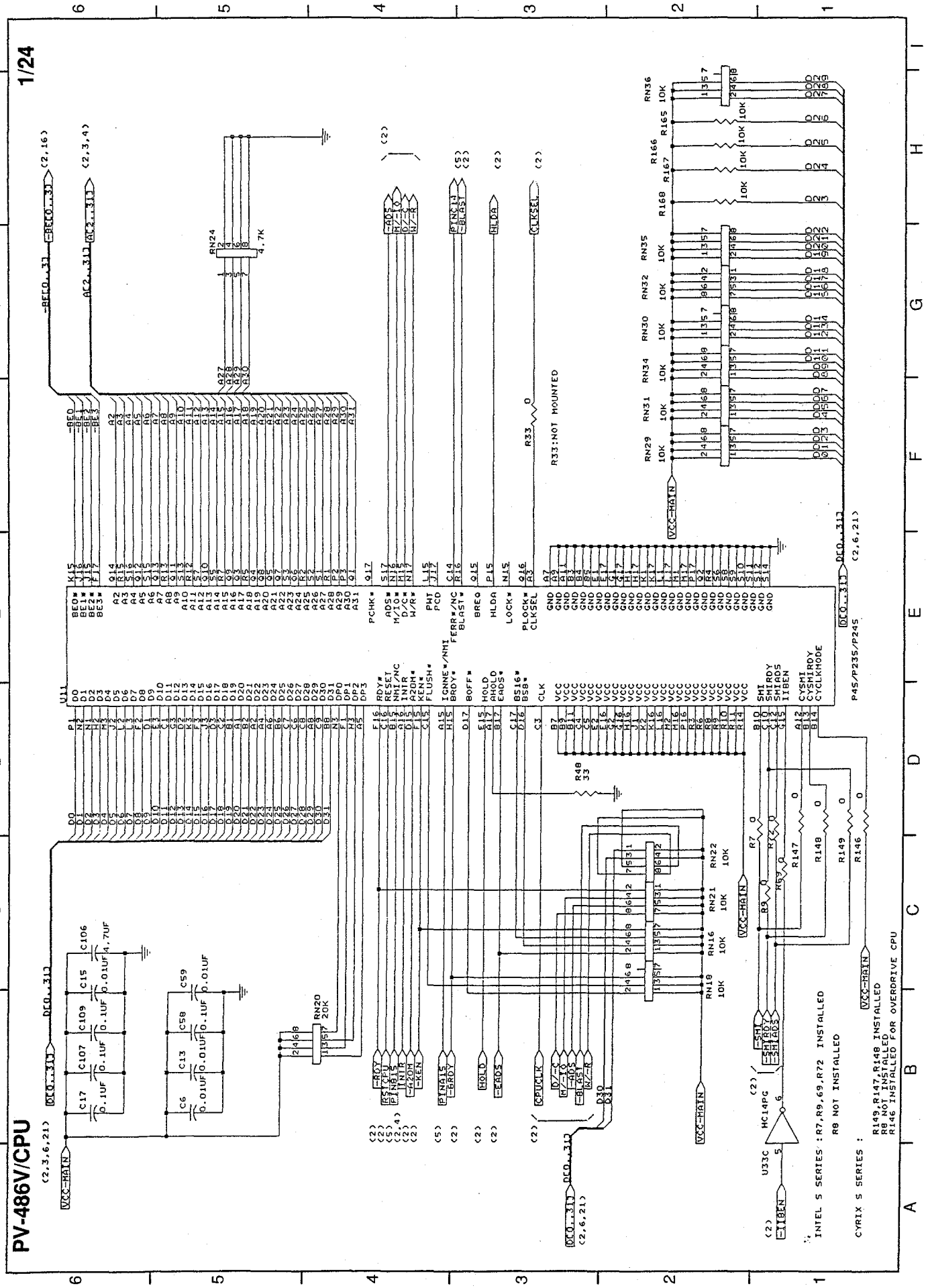
Checks that data can be read from the hard disk without errors. The test stops if an error is detected and displays an error message.

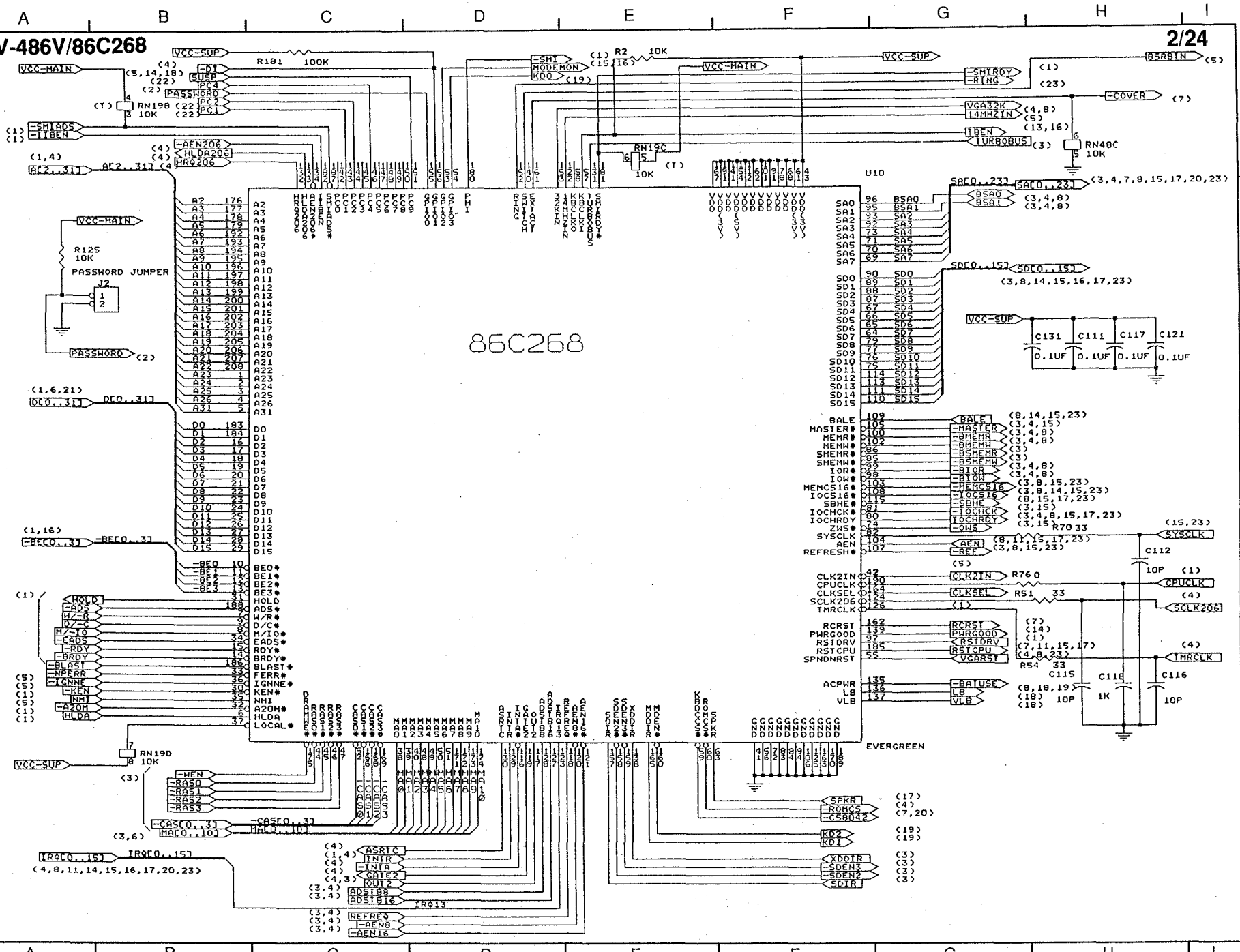
Write-read Check

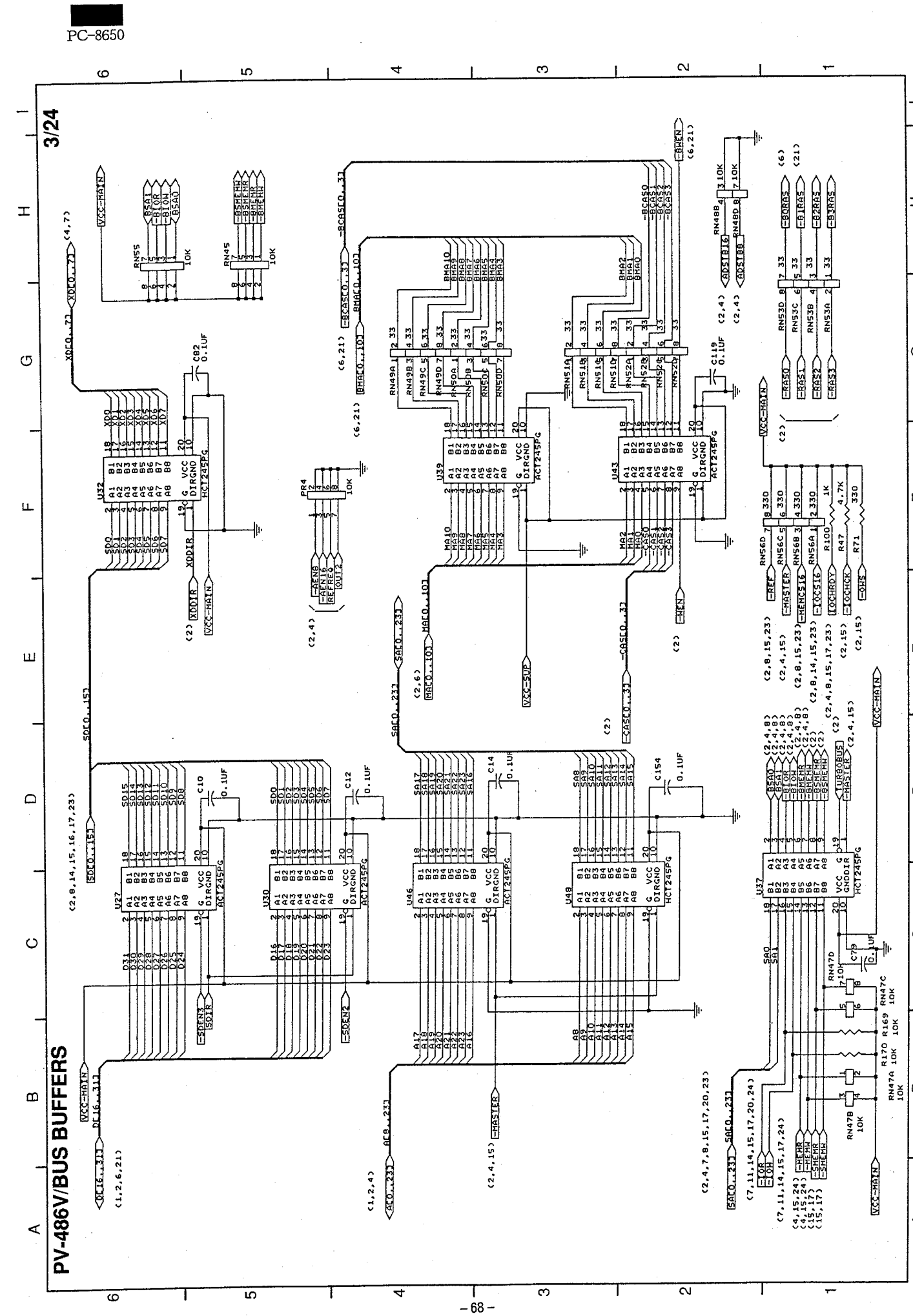
Checks if data can be written/read correctly by comparing data written to the hard disk with data read from the hard disk. This test destroys all existing data on the disk. The test stops if an error is detected and displays an error message. Do not run this test unless you have reason to believe there is a problem with your hard disk.

CHAPTER7. CIRCUIT DIAGRAM & PARTS LAYOUT

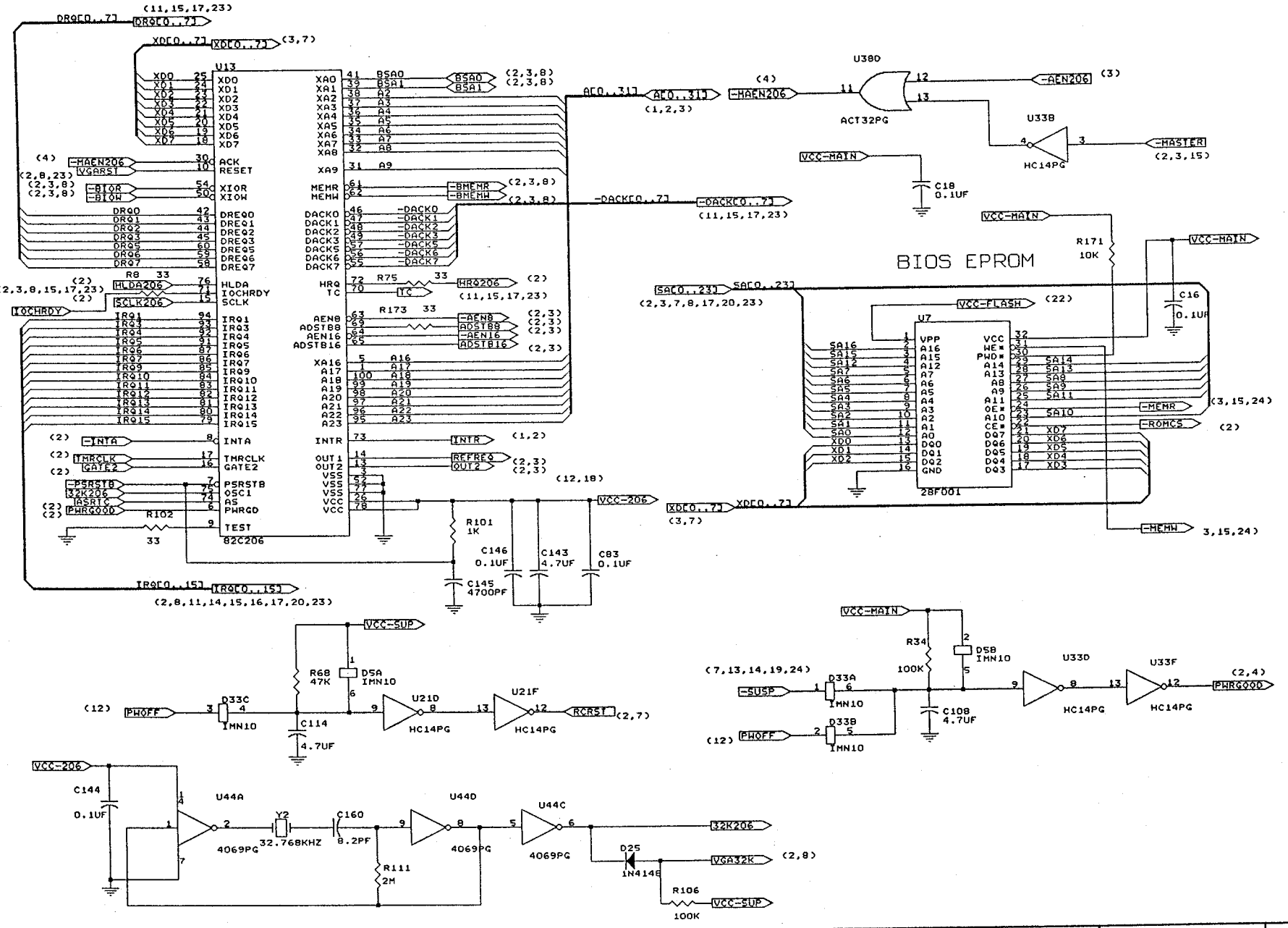
PV-486V/CPU

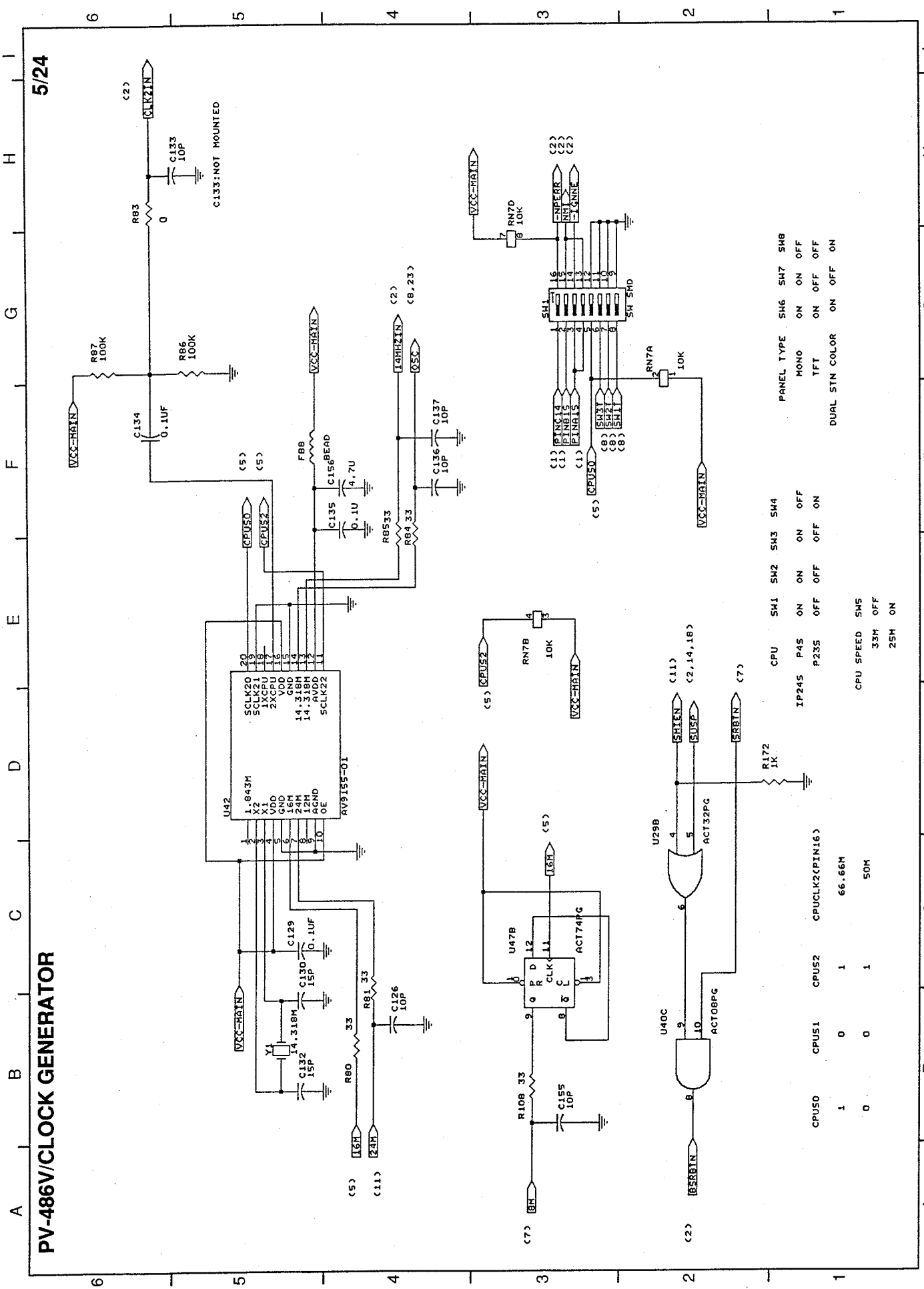


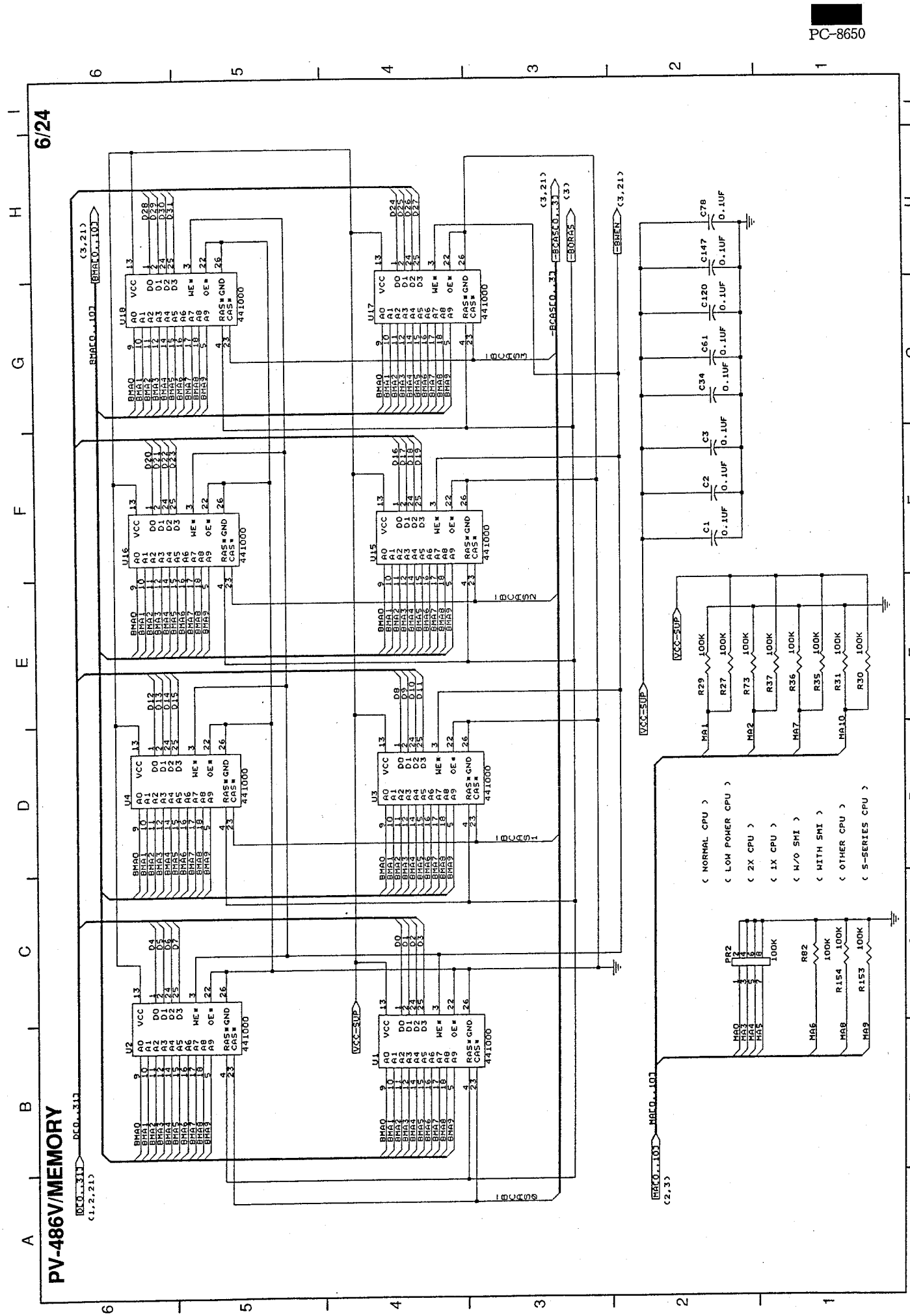

86C268
U10
EVERGREEN
VCC-SUP
VCC-MAIN
R101 100K
R125 10K
PASSWORD JUMPER
J2
PASSWORD
R2 10K
RN19B 10K
RN19C 10K
RN19D 10K
RN48C 10K
R70 33
R76 0
R51 33
R54 33
C131 0.1UF
C111 0.1UF
C117 0.1UF
C121 0.1UF
C112 10P
C115 10P
C116 1K
C116 10P
-SMI
MODEMON
KDQ
-SMIROY
-RING
-COVER
VGA32K
14MHZIN
IBEN
TURBOBUS
-AEN206
HLDA206
HRQ206
BSRBIN
BSA0
BSA1
SA0..23
SD0..15
BALE
-MASTER
-BMEMR
-BMEMW
-BSMEMR
-BSMEMW
-BIOR
-BIOW
-MEMCS16
-IOCS16
-SBHE
IOCHCK
IOCHRDY
-0WS
AEN
-REF
SYSCLK
CPUCLK
CLK2IN
CLKSEL
SCLK206
TMRCLK
RCRST
PURGOOD
-RSTDRV
RSTCPU
-VGARST
-BATUSE
LB
VLB
SPKR
-ROMCS
-CS8042
KD2
KD1
XDDIR
-SDEN1
-SDEN2
SDIR
-WEN
-RAS0
-RAS1
-RAS2
-RAS3
-CAS0..3
MA0..10
ASRTC
INTR
-INTA
GATE2
OUT2
ADS188
ADS816
IRQ13
REFRES
-AEN8
-AEN16
IRQ0..15
HOLD
-ADS
W/-R
D/-C
M/-IO
-EADS
-RDY
-BRDY
-BLAST
-NPERR
-IGNNE
-KEN
NMI
-A20M
HLDA
LOCAL
HLDA
BE0..3
BE0#
BE1#
BE2#
BE3#
ADS#
W/R#
D/C#
M/IO#
EADS#
RDY#
BRDY#
BLAST#
FERR#
IGNNE#
KEN#
NMI
A20M#
HLDA
LOCAL#

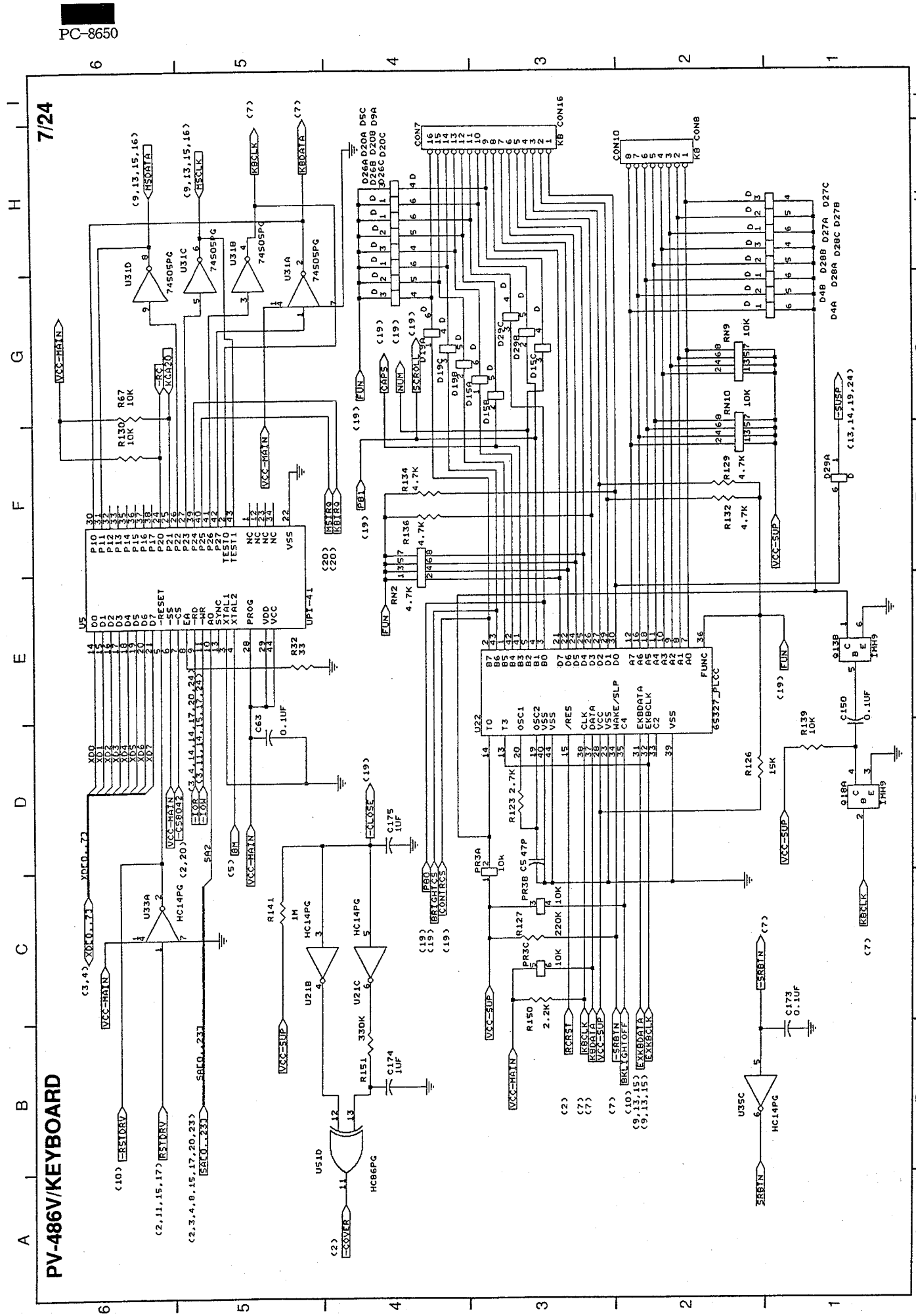

PV-486V/BUS BUFFERS
3/24

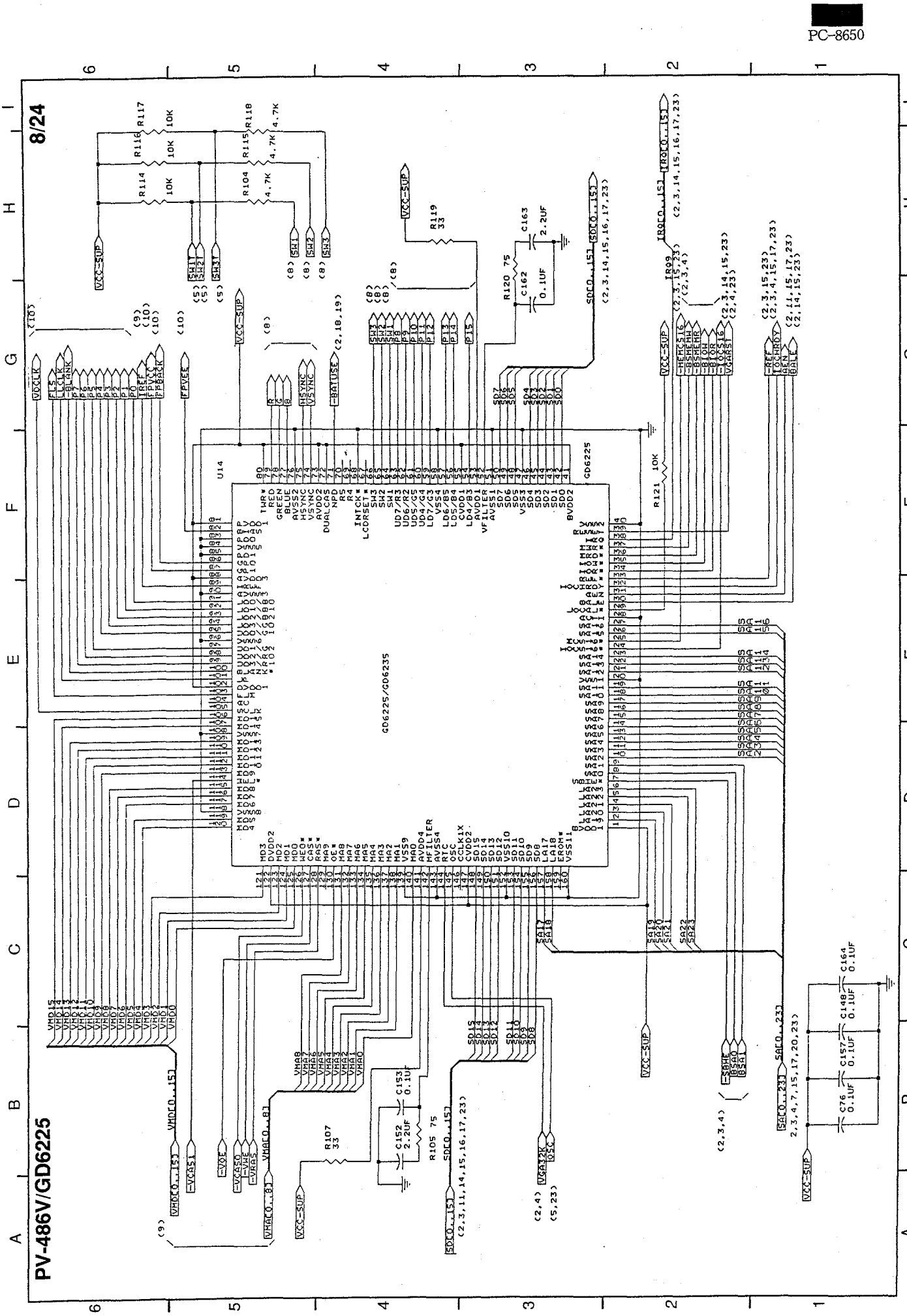
PV-486V/PERIPHERAL CONTROLLER/FLASH ROM

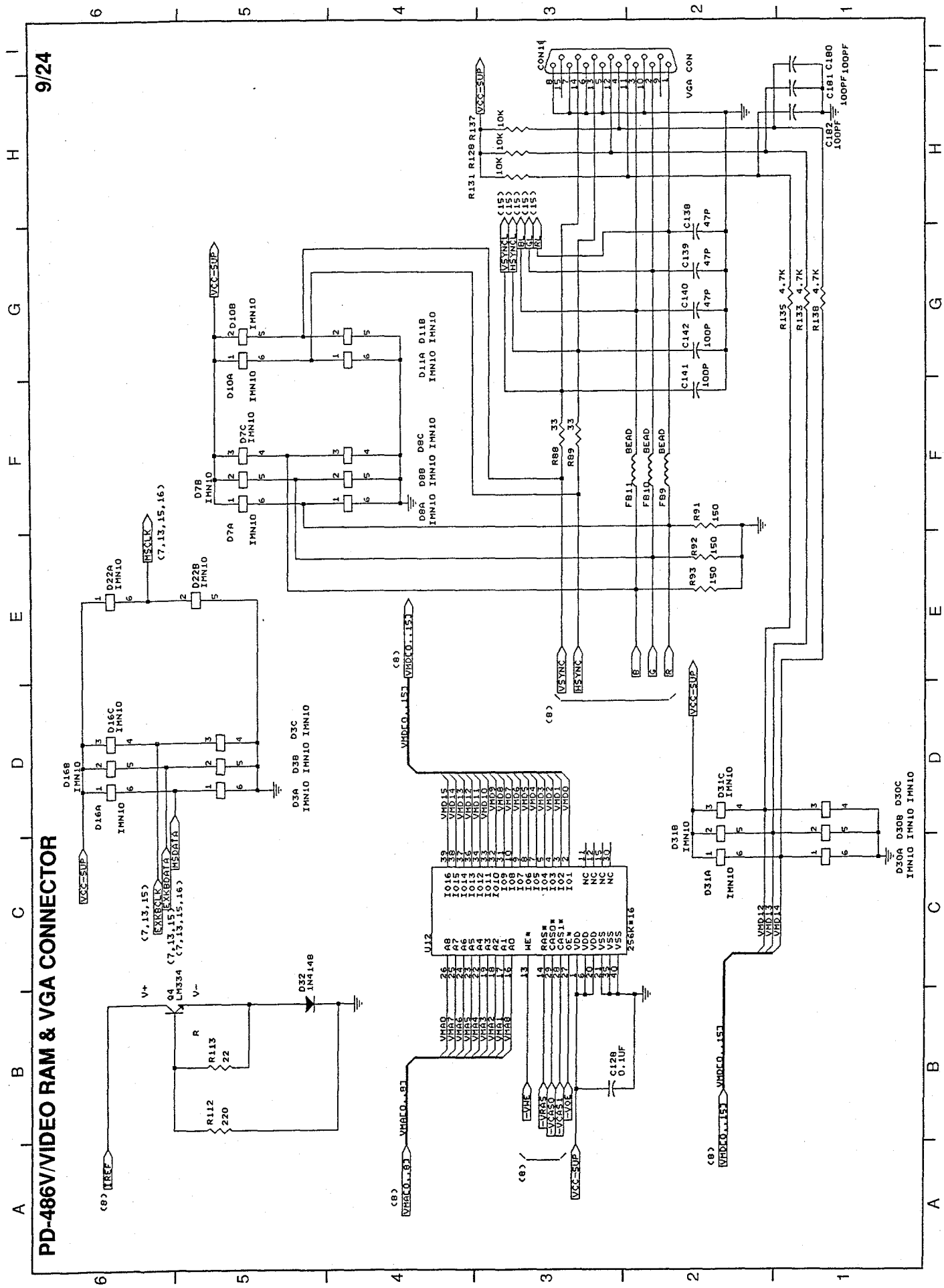


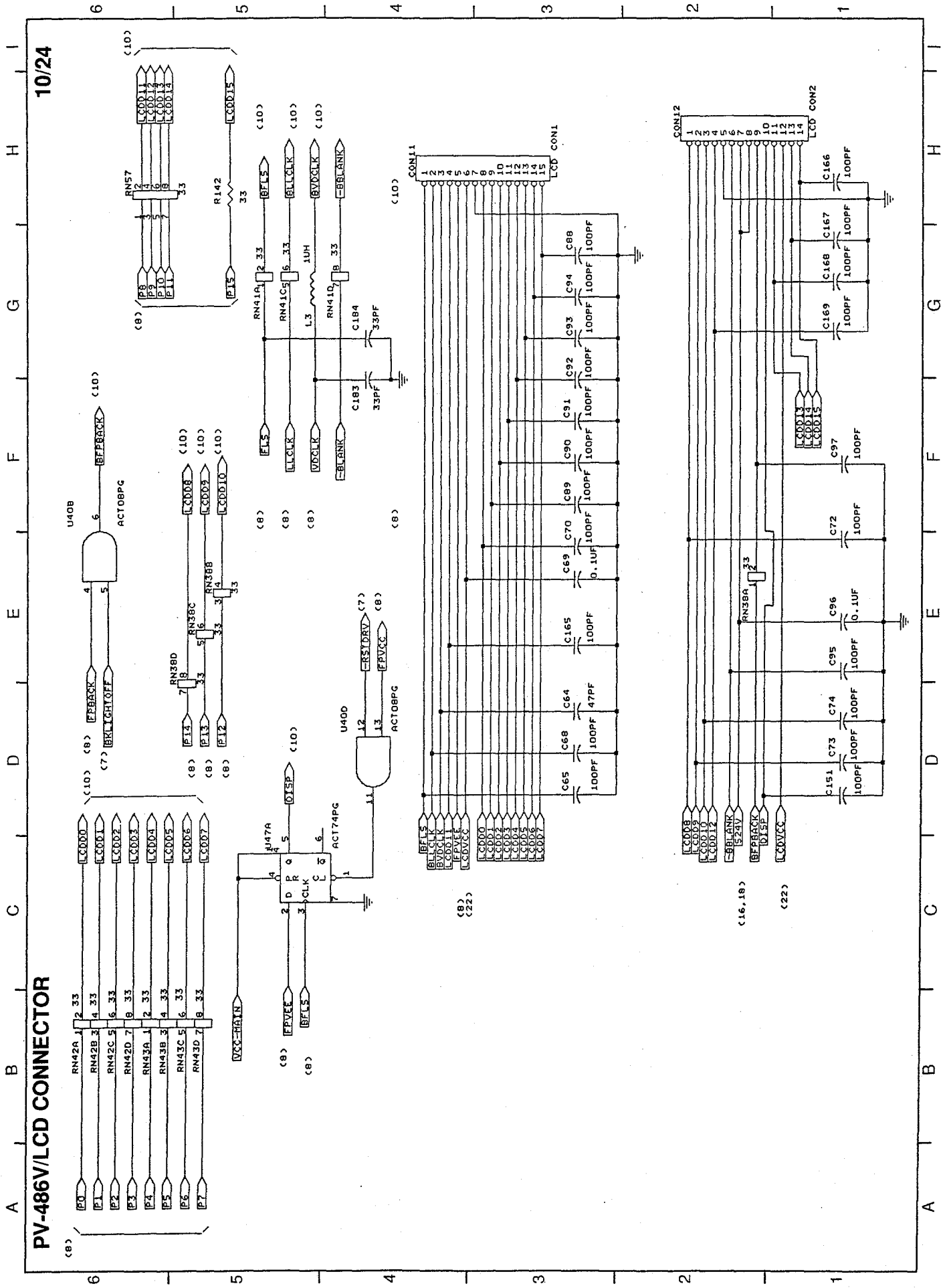

PV-486V/CLOCK GENERATOR
5/24
C133:NOT MOUNTED
U42
AV9155-01
U47B
ACT74PG
U29B
ACT32PG
U40C
ACT08PG
Y1
14.318M
CPU50 CPU51 CPU52 CPUCLK2(PIN16)
1 0 1 66.66M
0 0 1 50M
PANEL TYPE SW6 SW7 SW8
MONO ON ON OFF
TFT ON OFF OFF
DUAL STN COLOR ON OFF ON
CPU SW1 SW2 SW3 SW4
IP245 P4S ON ON ON OFF
P23S OFF OFF OFF ON
CPU SPEED SW5
33M OFF
25M ON


PV-486V/MEMORY
6/24
< NORMAL CPU >
< LOW POWER CPU >
< 2X CPU >
< 1X CPU >
< W/O SMI >
< WITH SMI >
< OTHER CPU >
< S-SERIES CPU >

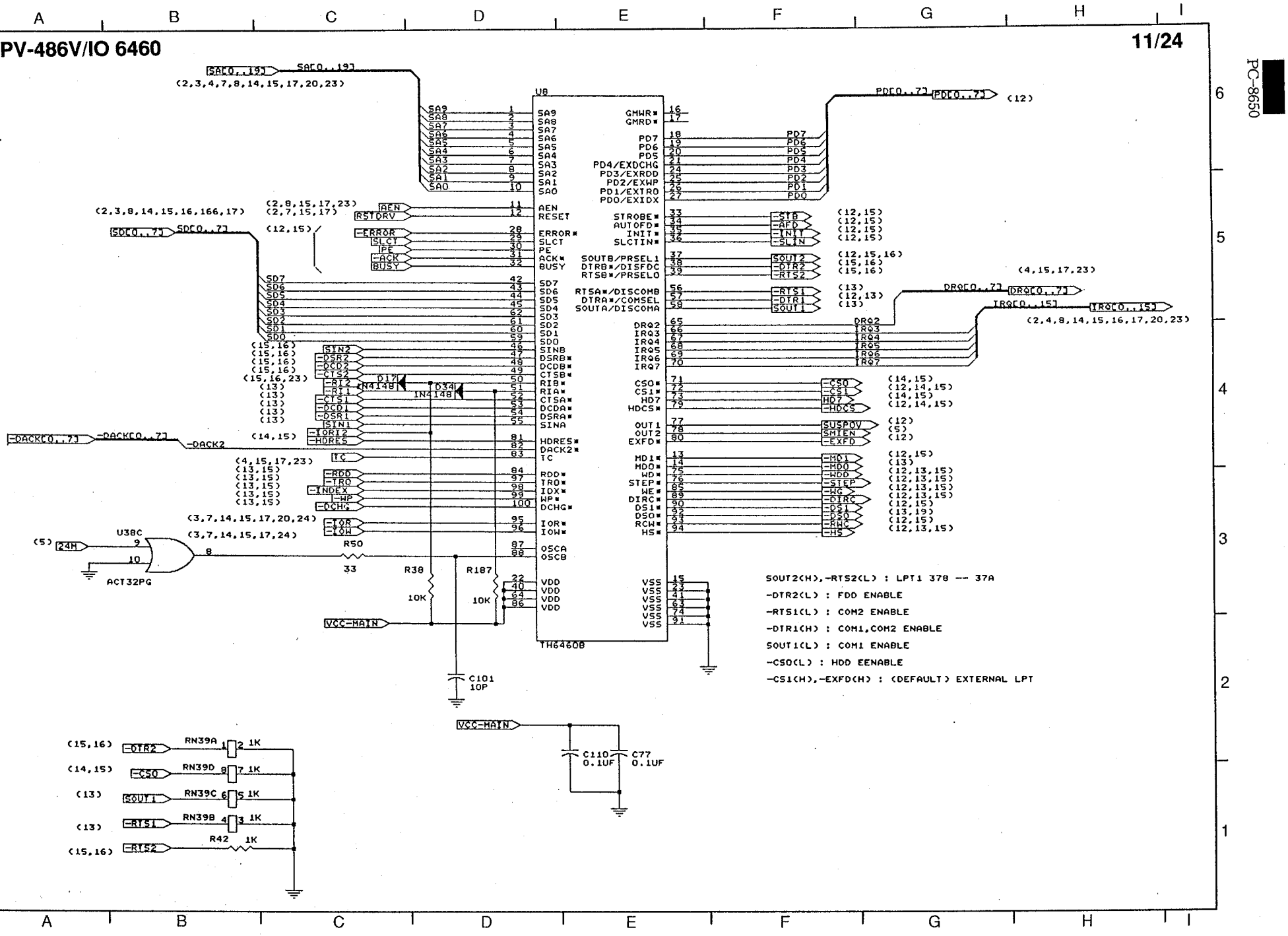

PV-486V/KEYBOARD
7/24
U5
UPI-41
U22
65327_PLCC
FUNC
U31A
U31B
U31C
U31D
74S05PG
U33A
HC14PG
U21B
U21C
U51D
HC86PG
U35C
Q18A
Q18B
Q13B
IMH9
CON7
KB CON16
CON10
KB CON8
RN2
RN9
RN10
R67 10K
R130 10K
R134 4.7K
R136 4.7K
R129 4.7K
R132 4.7K
R32 33
R141 1M
R151 330K
R123 2.7K
R127 220K
R150 2.2K
R126 15K
R139 10K
PR3A 10K
PR3B 10K
PR3C 10K
C47P
C63 0.1UF
C150 0.1UF
C173 0.1UF
C174 1UF
C175 1UF
D15A
D15B
D15C
D19A
D19B
D19C
D23A
D23B
D23C
D29A
D4A D28A D28C D27B
D4B D28B D27A D27C
D26A D20A DSC
D26B D20B D9A
D26C D20C
VCC-MAIN
VCC-SUP
-SUSP
-RESET
-CS
EA
-RD
-WR
ALE
SYNC
XTAL1
XTAL2
PROG
VDD
VCC
VSS
TEST0
TEST1
MSIRQ
KBIRQ
FUN
CAPS
NUM
SCROLL
PB1
PB0
BRTGHTCS
CONTRCS
-CLOSE
-COVER
-CSB042
-IOR
-IOW
SA2
SA0..23
XD0..7
RSTDRV
KBCLK
KBDATA
HSDATA
HSCLK
RCRST
EXKBDATA
EXKBCLK
BKLIGHTOFF
-SRBIN
SRBIN

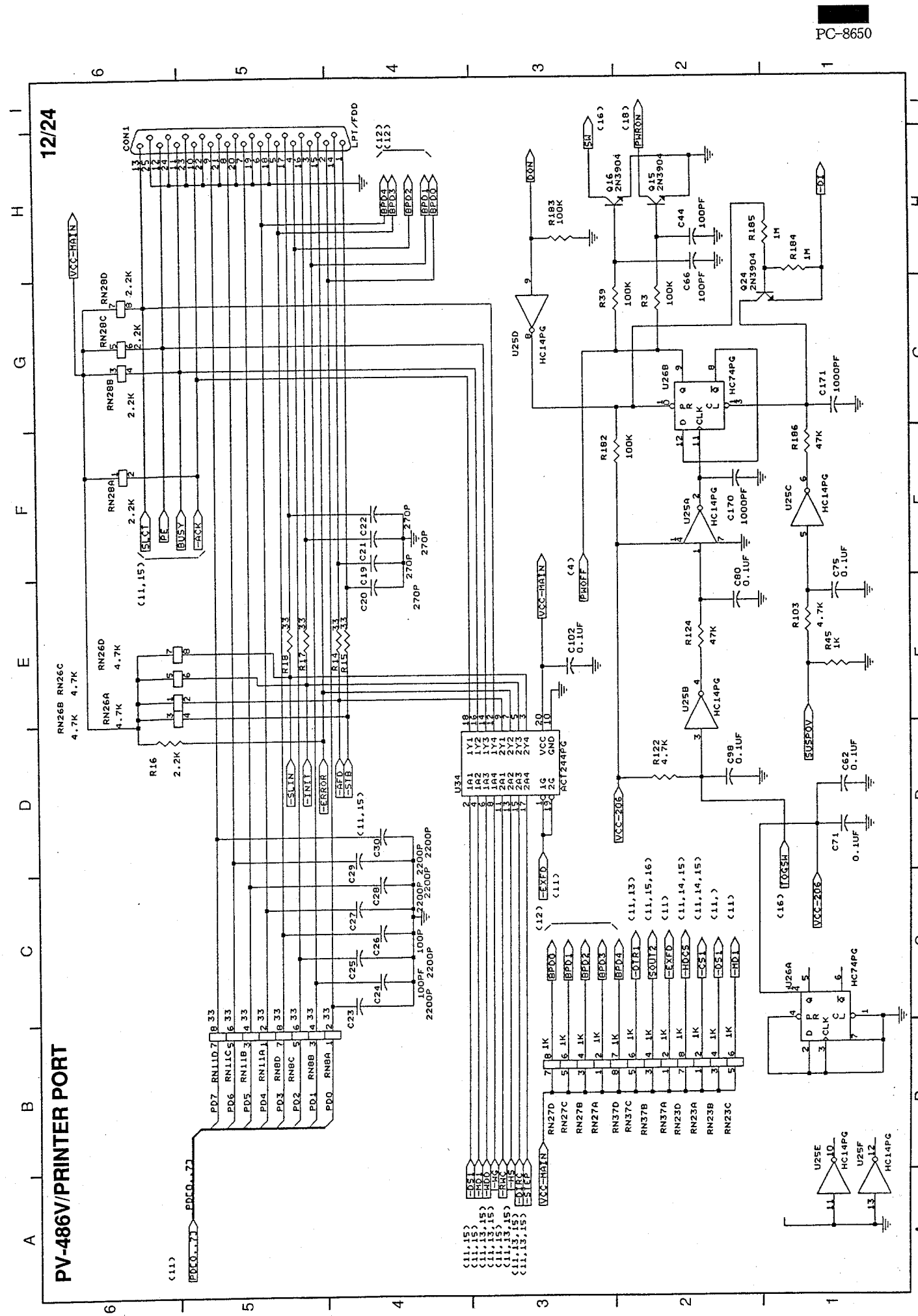

PV-486V/GD6225
8/24
GD6225/GD6235
U14
GD6225
VCC-SUP
VGCLK
VHD15
VHD14
VHD13
VHD12
VHD11
VHD10
VHD9
VHD8
VHD7
VHD6
VHD5
VHD4
VHD3
VHD2
VHD1
VHD0
VHDCO..15
VHDCO..8
-VCAS1
-VOE
-VCAS0
-VWE
-VRAS
VHA8
VHA7
VHA6
VHA5
VHA4
VHA3
VHA2
VHA1
VHA0
R107 33
C153 0.1UF
C152 2.2UF
R105 75
SDCO..15
VGA32K
OSC
SD15
SD14
SD13
SD12
SD11
SD10
SD9
SD8
SA17
SA18
SA19
SA20
SA21
SA22
SA23
SA0
SA1
-SBHE
-MEMCS16
-BSMEMW
-BSMEMR
-BIOCHRDY
-IOCS16
VGARST
IRQCO..15
R119 33
R120 75
C162 0.1UF
C163 2.2UF
R121 10K
R114 10K
R116 10K
R117 10K
R104 4.7K
R115 4.7K
R118 4.7K
SW1
SW2
SW3
SW31
-BATUSE
C76 0.1UF
C157 0.1UF
C148 0.1UF
C164 0.1UF

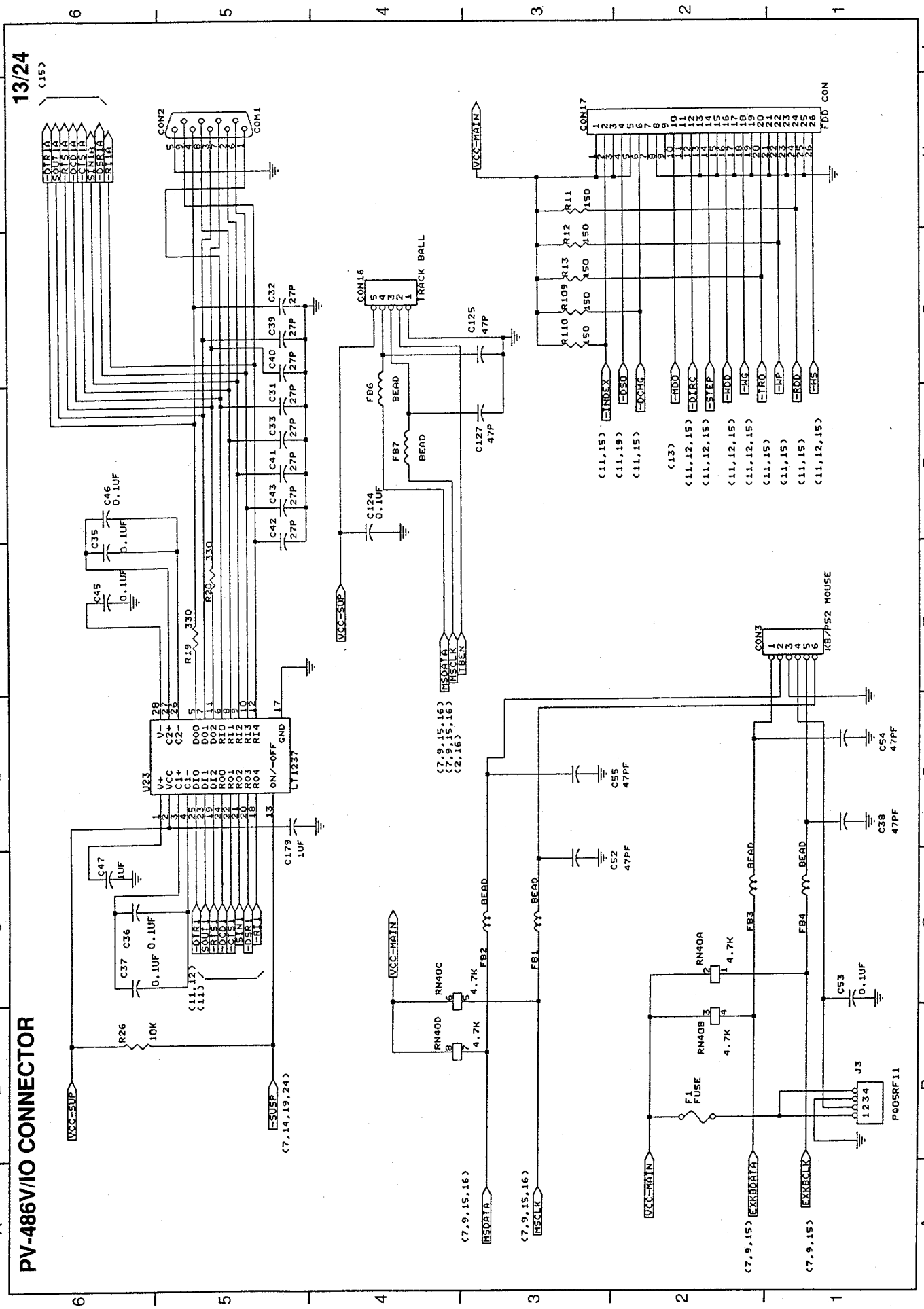

PD-486V/VIDEO RAM & VGA CONNECTOR
9/24
VGA CON
CON14
U12
256K*16
Q4
LM334
D32
1N4148
R112
220
R113
22
C128
0.1UF
R88
33
R89
33
FB11
BEAD
FB10
BEAD
FB9
BEAD
R91
150
R92
150
R93
150
R135
4.7K
R133
4.7K
R138
4.7K
R131
10K
R128
10K
R137
10K
C138
47P
C139
47P
C140
47P
C142
100P
C141
100P
C181
100PF
C180
100PF
C182
100PF
VCC-5UP
VSYNC
HSYNC
MSCLK
MSDATA
EXKBCLK
EXKBDATA
IREF
VMD0..15
VMA0..8
D10A
D10B
D11A
D11B
D7A
D7B
D7C
D8A
D8B
D8C
D22A
D22B
D16A
D16B
D16C
D3A
D3B
D3C
D31A
D31B
D31C
D30A
D30B
D30C
IMN10

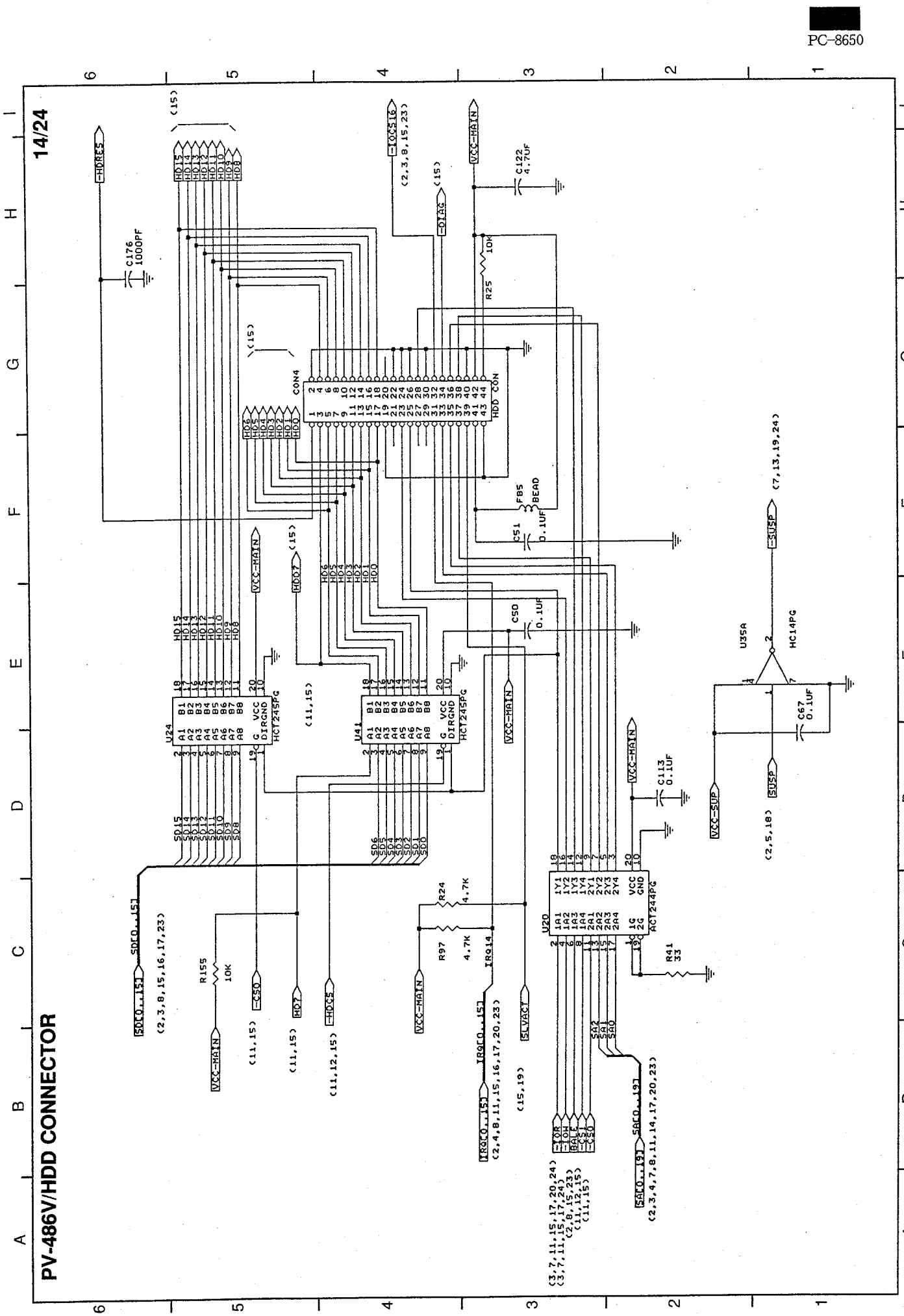

PV-486V/LCD CONNECTOR
10/24

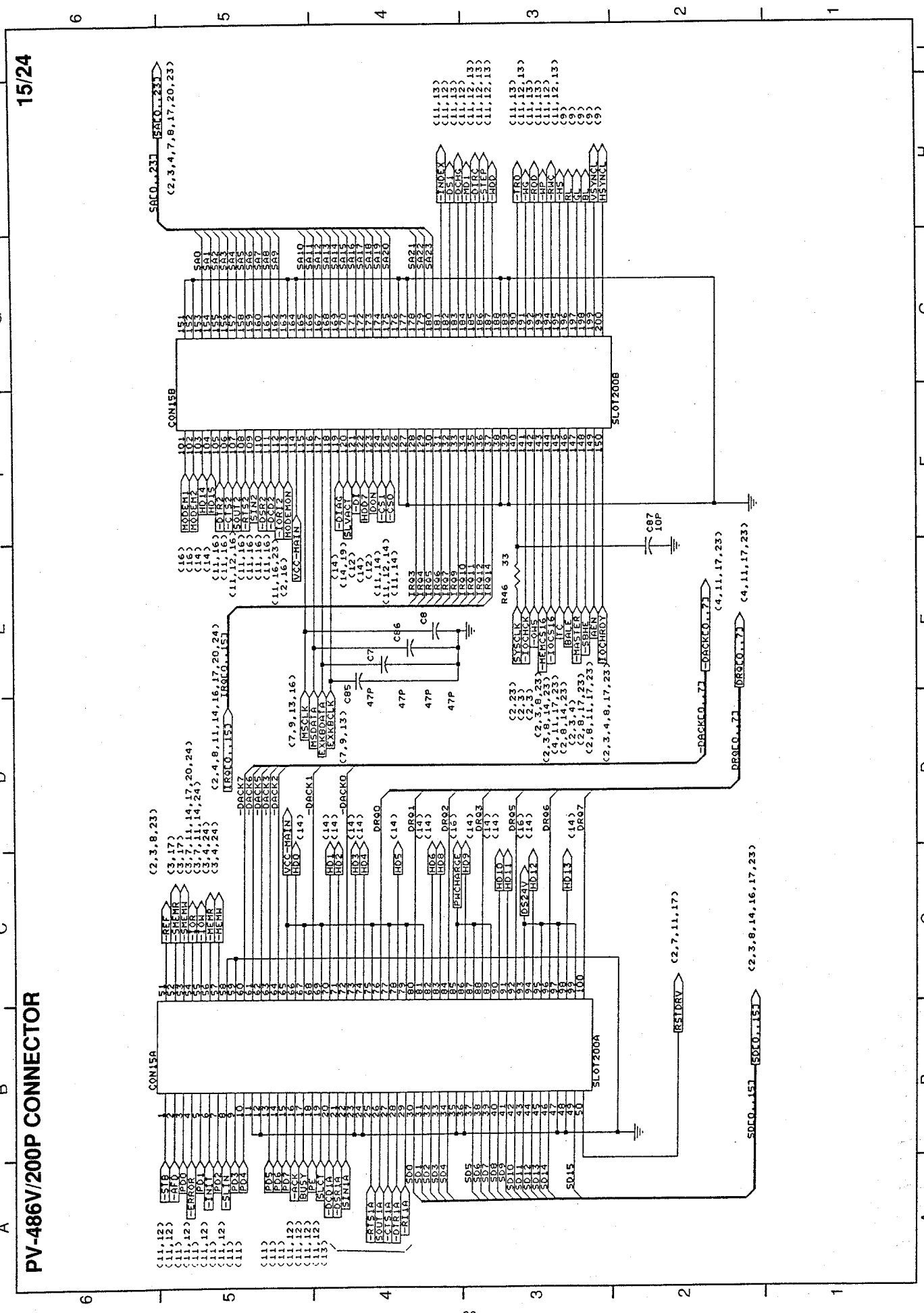
PV-486V/IO 6460

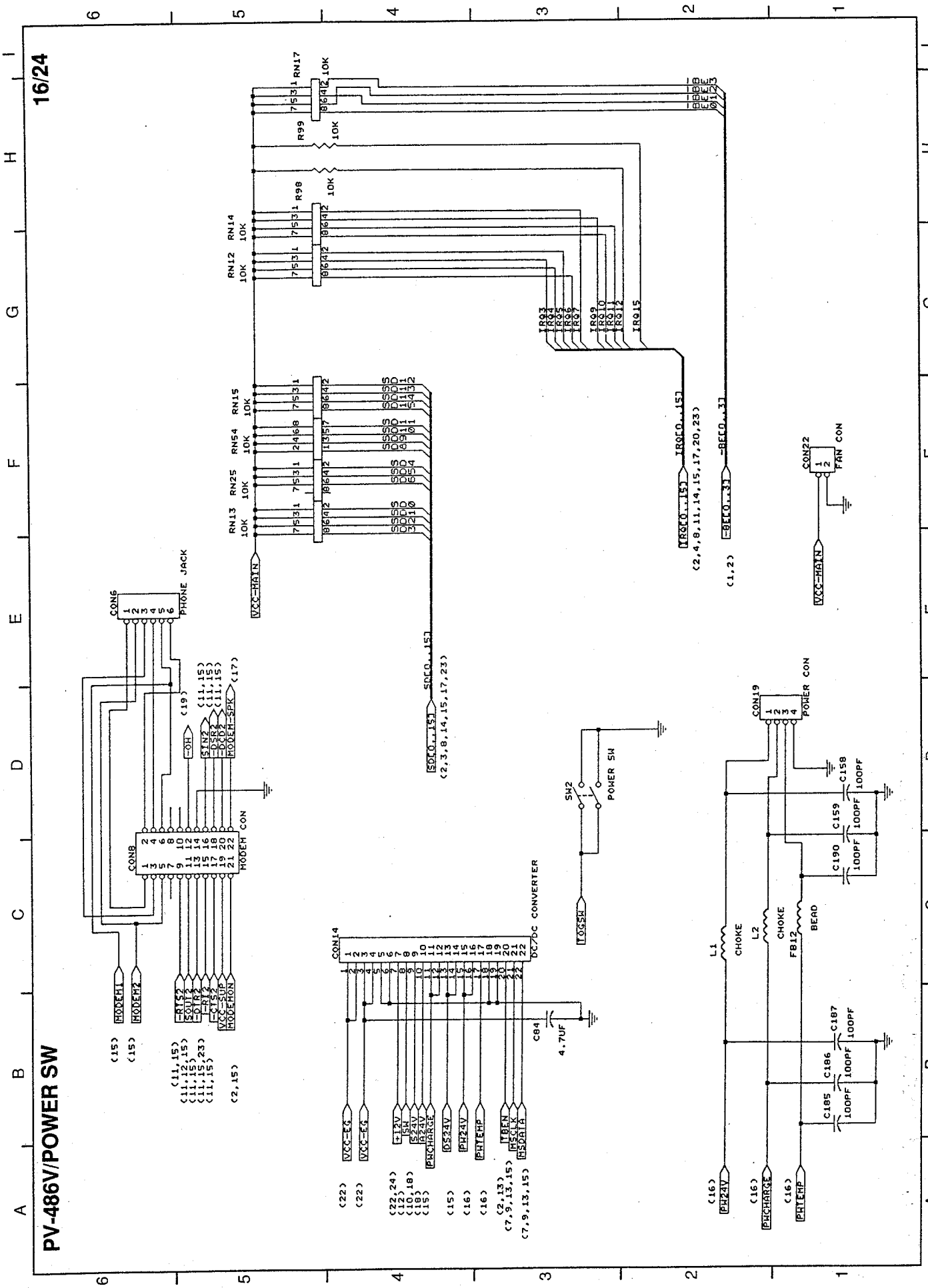



PV-486V/PRINTER PORT
12/24
VCC-MAIN
CON1
LPT/FDD
RN28D 2.2K
RN28C 2.2K
RN28B 2.2K
RN28A 2.2K
RN26B RN26C 4.7K 4.7K
RN26A 4.7K
RN26D 4.7K
R16 2.2K
R18 33
R17 33
R14 33
R15 33
SLCT
PE
BUSY
-ACK
-SLIN
-INIT
-ERROR
-AFD
-STB
U34 ACT244PG
C102 0.1UF
C19 C20 C21 C22 270P
C23 C24 C25 C26 C27 C28 C29 C30 100PF 2200P
RN11D RN11C RN11B RN11A RN8D RN8C RN8B RN8A 33
PD7 PD6 PD5 PD4 PD3 PD2 PD1 PD0
PDD0..7
BPD0 BPD1 BPD2 BPD3 BPD4
RN27D RN27C RN27B RN27A RN37D RN37C RN37B RN37A RN23D RN23A RN23B RN23C 1K
-OTR1 -STOUT2 -EXFD -HDIS -CS1 -DS1 -HD1
-EXFD
VCC-MAIN
VCC-206
U25D HC14PG
U25A HC14PG
U25B HC14PG
U25C HC14PG
U25E HC14PG
U25F HC14PG
U26A HC74PG
U26B HC74PG
R183 100K
R182 100K
R124 47K
R122 4.7K
R39 100K
R3 100K
R186 47K
R103 4.7K
R45 1K
R184 1M
R185 1M
Q16 2N3904
Q15 2N3904
Q24 2N3904
C44 100PF
C66 100PF
C171 1000PF
C170 1000PF
C80 0.1UF
C98 0.1UF
C75 0.1UF
C62 0.1UF
C71 0.1UF
PWOFF
PWRON
SUSPOV
TOGSW
CON
SW
-D1


PV-486V/IO CONNECTOR
13/24
CON2
COM1
CON16
TRACK BALL
CON17
FDD CON
CON3
KB/PS2 MOUSE
U23
LT1237
J3
P005RF11
F1
FUSE
VCC-MAIN
VCC-5UP
-5USP
HSDATA
HSCLK
EXKBDATA
EXKBCLK
-DTR1
-SOUT1
-RTS1
-DCD1
-CTS1
-DSR1
-RI1
-DIR
-STEP
-HDD
-WG
-TRO
-WP
-RDD
-HS
-INDEX
-DSO
-DCHG
R19 330
R20 330
R26 10K
R109 150
R110 150
R11 150
R12 150
R13 150
FB1 BEAD
FB2 BEAD
FB3 BEAD
FB4 BEAD
FB6 BEAD
FB7 BEAD
RN40A 4.7K
RN40B 4.7K
RN40C 4.7K
RN40D 4.7K
C125 47P
C127 47P
C124 0.1UF
C53 0.1UF
C54 47PF
C55 47PF
C52 47PF
C38 47PF
C179 1UF
C47 1UF
C46 0.1UF
C35 0.1UF
C45 0.1UF
C36 0.1UF
C37 0.1UF
C32 27P
C39 27P
C40 27P
C31 27P
C33 27P
C41 27P
C43 27P
C42 27P

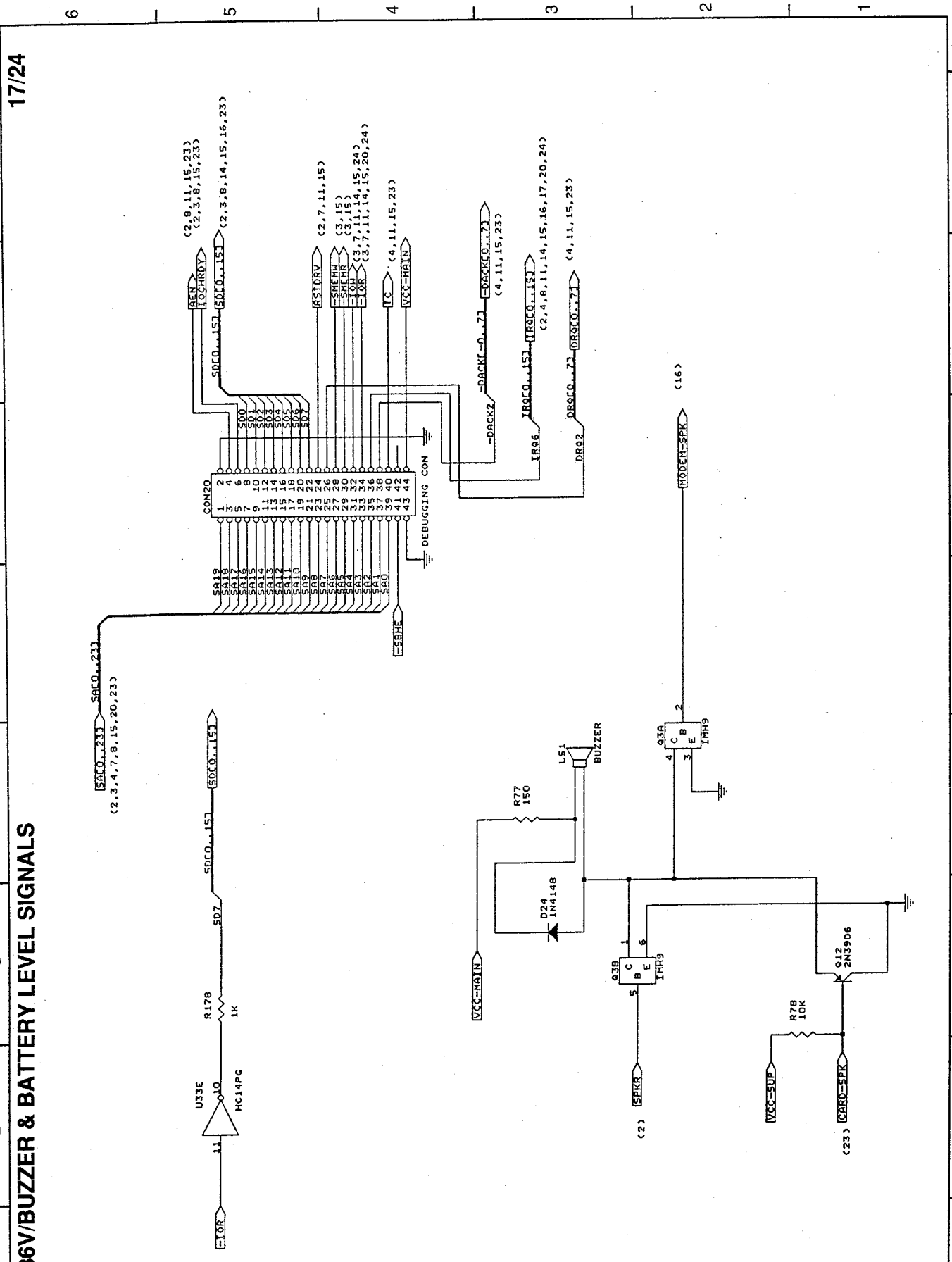

PV-486V/HDD CONNECTOR
14/24
-HDRES
C176 1000PF
HD15 HD14 HD13 HD12 HD11 HD10 HD9 HD8
HD6 HD5 HD4 HD3 HD2 HD1 HD0
CON4
HDD CON
-IOCS16
-DIAG
VCC-MAIN
C122 4.7UF
R25 10K
FB5 BEAD
C51 0.1UF
C50 0.1UF
U24
U41
HCT245PG
SD15 SD14 SD13 SD12 SD11 SD10 SD9 SD8
SD6 SD5 SD4 SD3 SD2 SD1 SD0
SDC0..15
R155 10K
-CS0
HD7
-HDCS
R24 4.7K
R97 4.7K
IR14
IRQC0..15
SLVACT
U20
ACT244PG
C113 0.1UF
R41 33
SA2 SA1 SA0
SAC0..19
-IOR
-IOW
BALE
-CS1
-CS0
U35A
HC14PG
C67 0.1UF
-SUSP
VCC-SUP
(2,3,8,15,16,17,23)
(11,15)
(11,12,15)
(15,19)
(2,4,8,11,15,16,17,20,23)
(2,3,4,7,8,11,14,17,20,23)
(3,7,11,15,17,20,24)
(3,7,11,15,17,24)
(2,8,15,23)
(11,12,15)
(11,15)
(7,13,19,24)
(2,5,18)

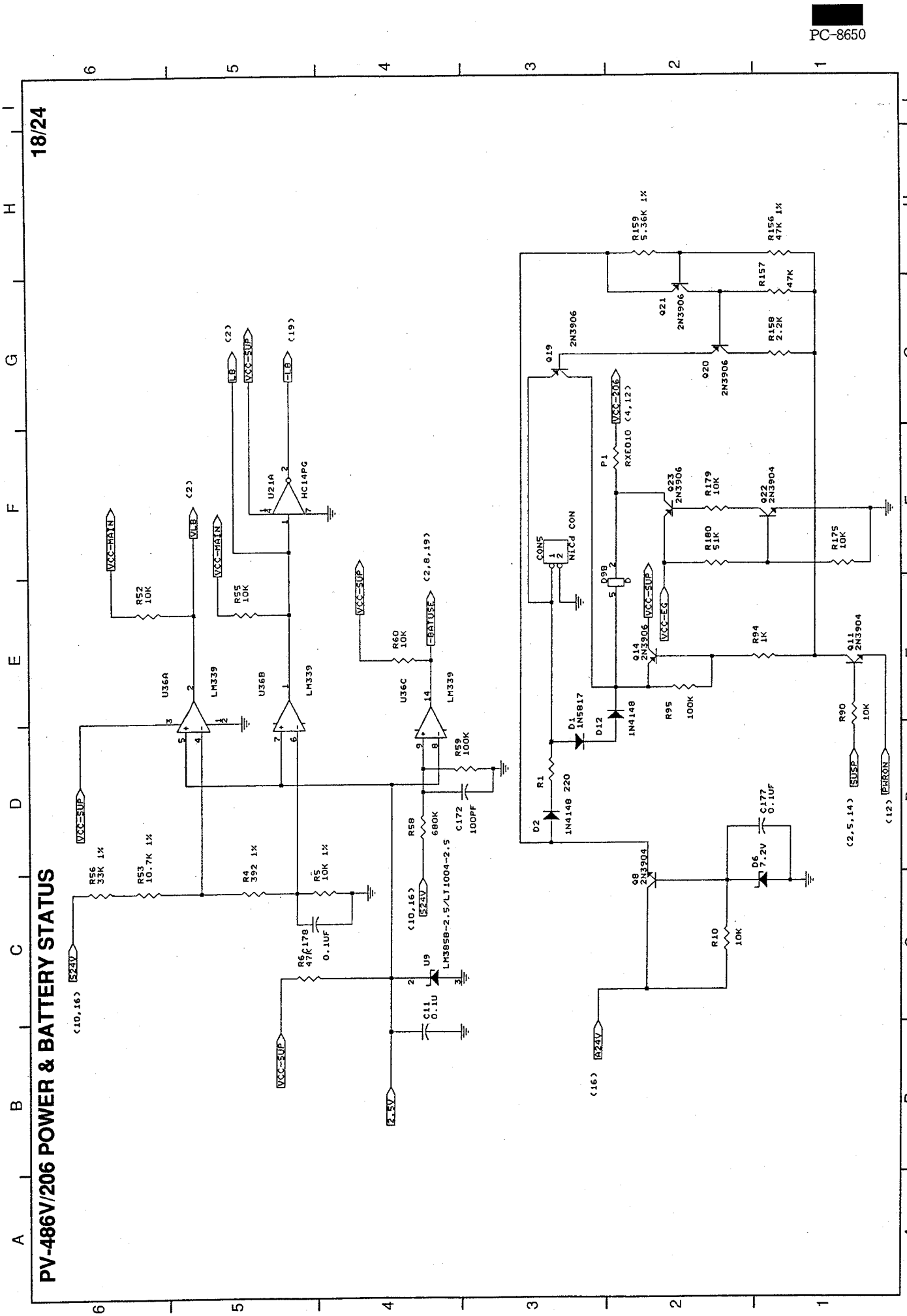

PV-486V/200P CONNECTOR
15/24
CON15A
SLOT200A
CON15B
SLOT200B

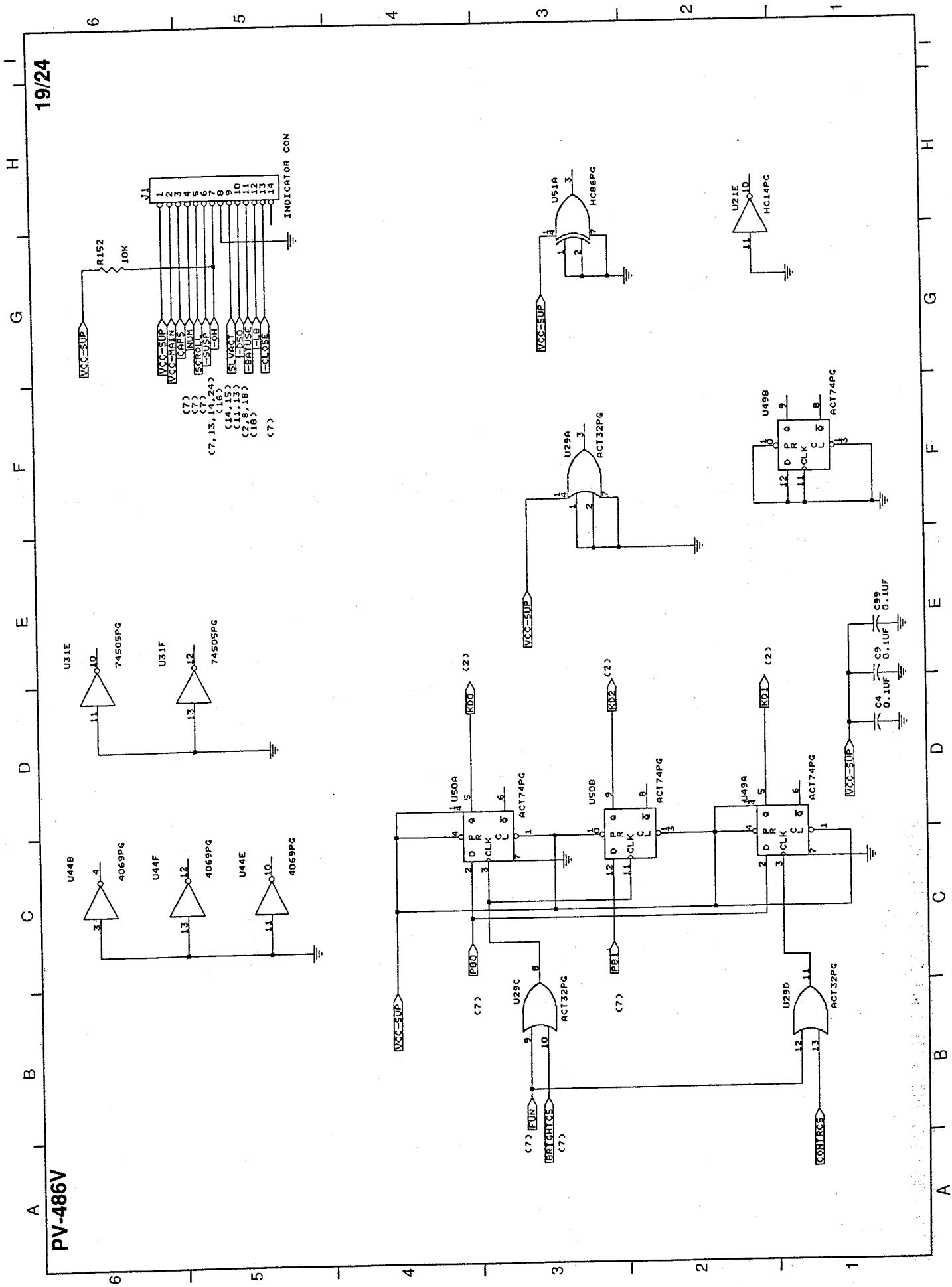

PV-486V/POWER SW
16/24
CON6
PHONE JACK
CON8
MODEM CON
MODEM1
MODEM2
-RTS2
SOUT2
-DTR2
SIN2
-DCD2
-CTS2
VCC-5V
MODEMON
-OH
MODEM-SPK
RN12 RN14 RN17 RN13 RN25 RN54 RN15
10K
R99
R98
VCC-MAIN
IRQ3
IRQ4
IRQ5
IRQ7
IRQ9
IRQ10
IRQ11
IRQ12
IRQ15
IRQ0..15
SDC0..15
-BEC0..3
CON14
DC/DC CONVERTER
VCC-EC
+12V
SW
S24V
A24V
PWCHARGE
PH24V
PHTEMP
-TBEN
MSCLK
MSDATA
C84
4.7UF
SW2
POWER SW
TOGSW
CON19
POWER CON
L1
L2
CHOKE
FB12
BEAD
C158
C159
C190
C185
C186
C187
100PF
CON22
FAN CON

PV-486V/BUZZER & BATTERY LEVEL SIGNALS

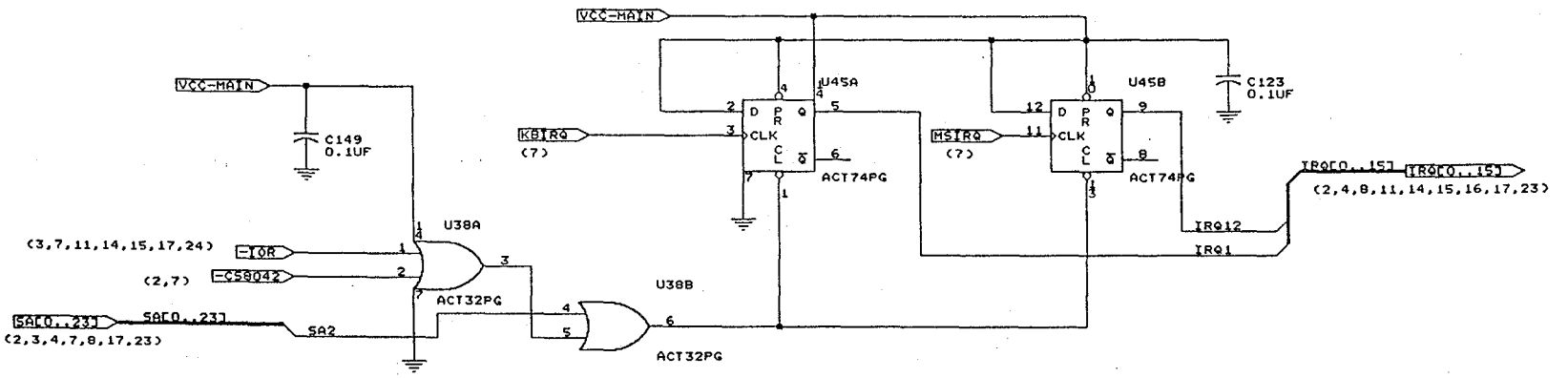
17/24

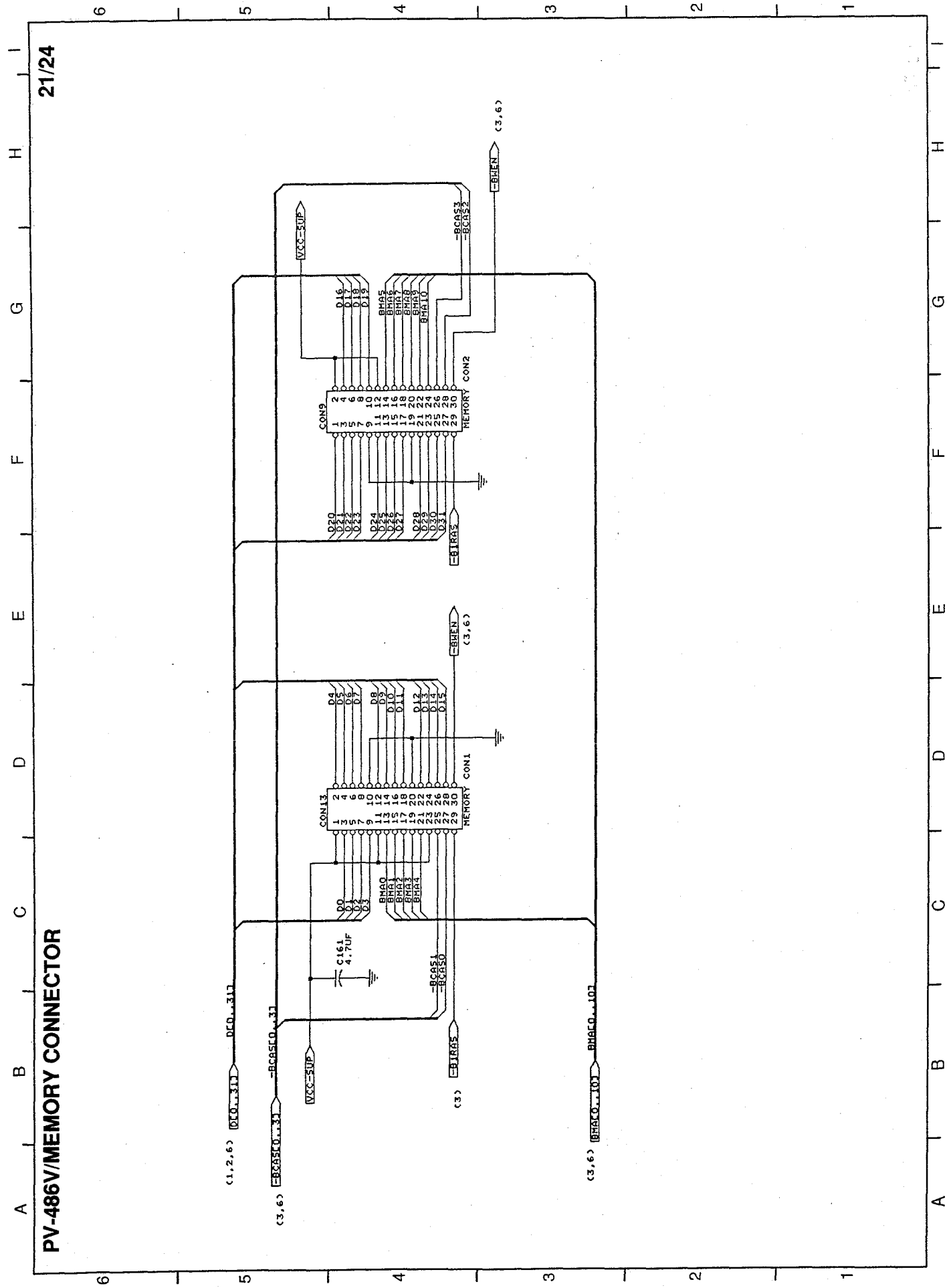



PV-486V/206 POWER & BATTERY STATUS
18/24
VCC-MAIN
VCC-SUP
VCC-206
VCC-EG
BATUSE
LB
CLB
SUSP
PSRON
U36A
U36B
U36C
LM339
U21A
HC14PG
U9
LM385B-2.5/LT1004-2.5
CON5
NICd CON
D98
P1
RXE010
Q19
Q20
Q21
Q22
Q23
Q14
Q11
Q8
2N3906
2N3904
D1
1N5817
D2
1N4148
D6
7.2V
D12
R1
220
R4
392 1%
R5
10K 1%
R10
10K
R52
10K
R53
10.7K 1%
R55
10K
R56
33K 1%
R58
680K
R59
100K
R60
10K
R90
10K
R94
1K
R95
100K
R156
47K 1%
R157
47K
R158
2.2K
R159
5.36K 1%
R175
10K
R179
10K
R180
5.1K
C11
0.1U
C172
100PF
C177
0.1UF
R6
47K 178
0.1UF
S24V
2.5V
(2)
(10,16)
(2,8,19)
(2,5,14)
(12)
(16)
(19)
(4,12)

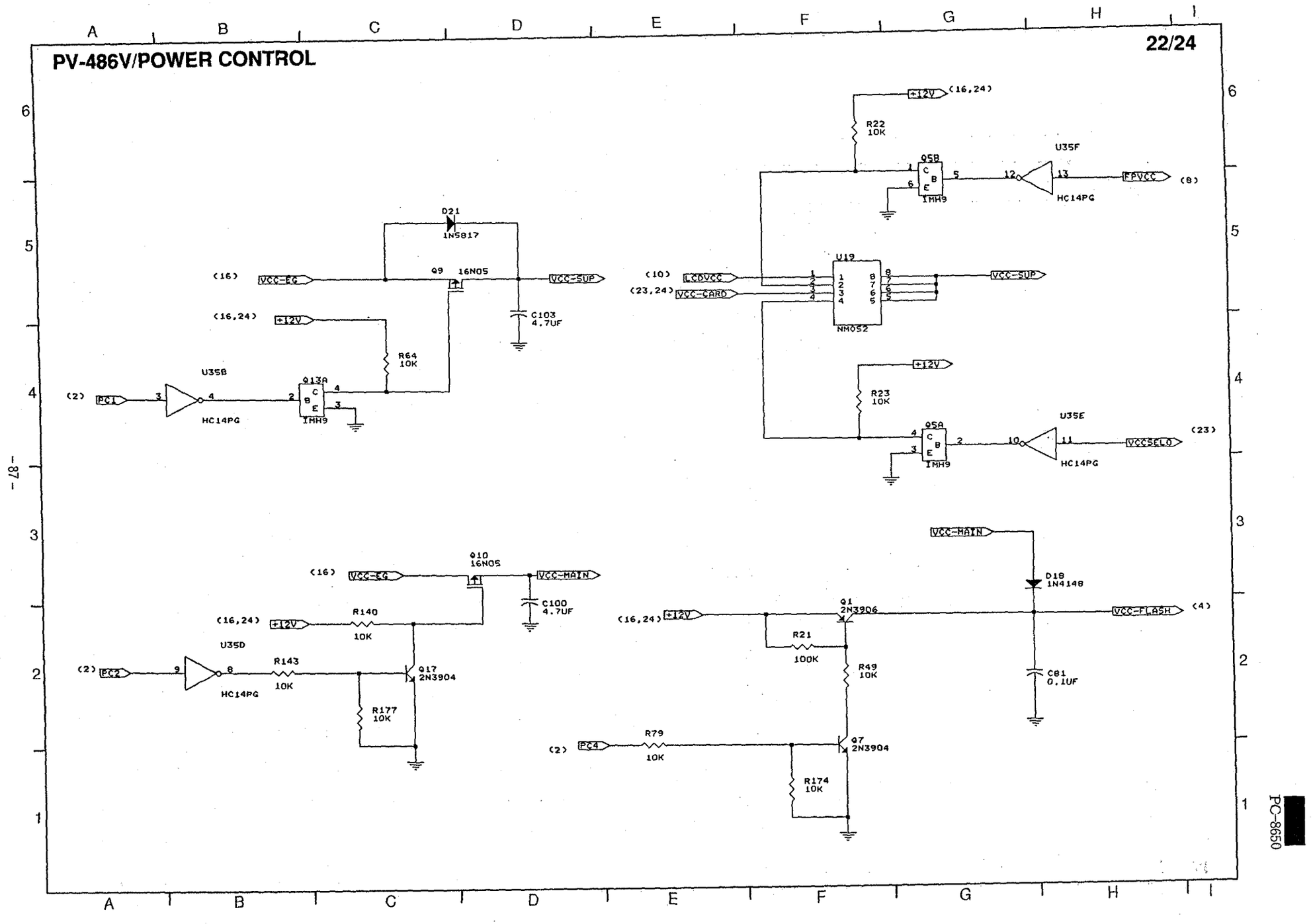

19/24
PV-486V
INDICATOR CON
R152
10K
VCC-SUP
VCC-MAIN
CAPS
NUM
SCROLL
-SUSP
-ON
SLVACT
-DSO
-BATUSE
-LB
-CLOSE
U31E
U31F
74S05PG
U44B
U44F
U44E
4069PG
U50A
U50B
U49A
U49B
ACT74PG
U29A
U29C
U29D
ACT32PG
U51A
HC86PG
U21E
HC14PG
KD0
KD1
KD2
PB0
PB1
FUN
BRIGHTCS
CONTRCS
C4
C9
C99
0.1UF

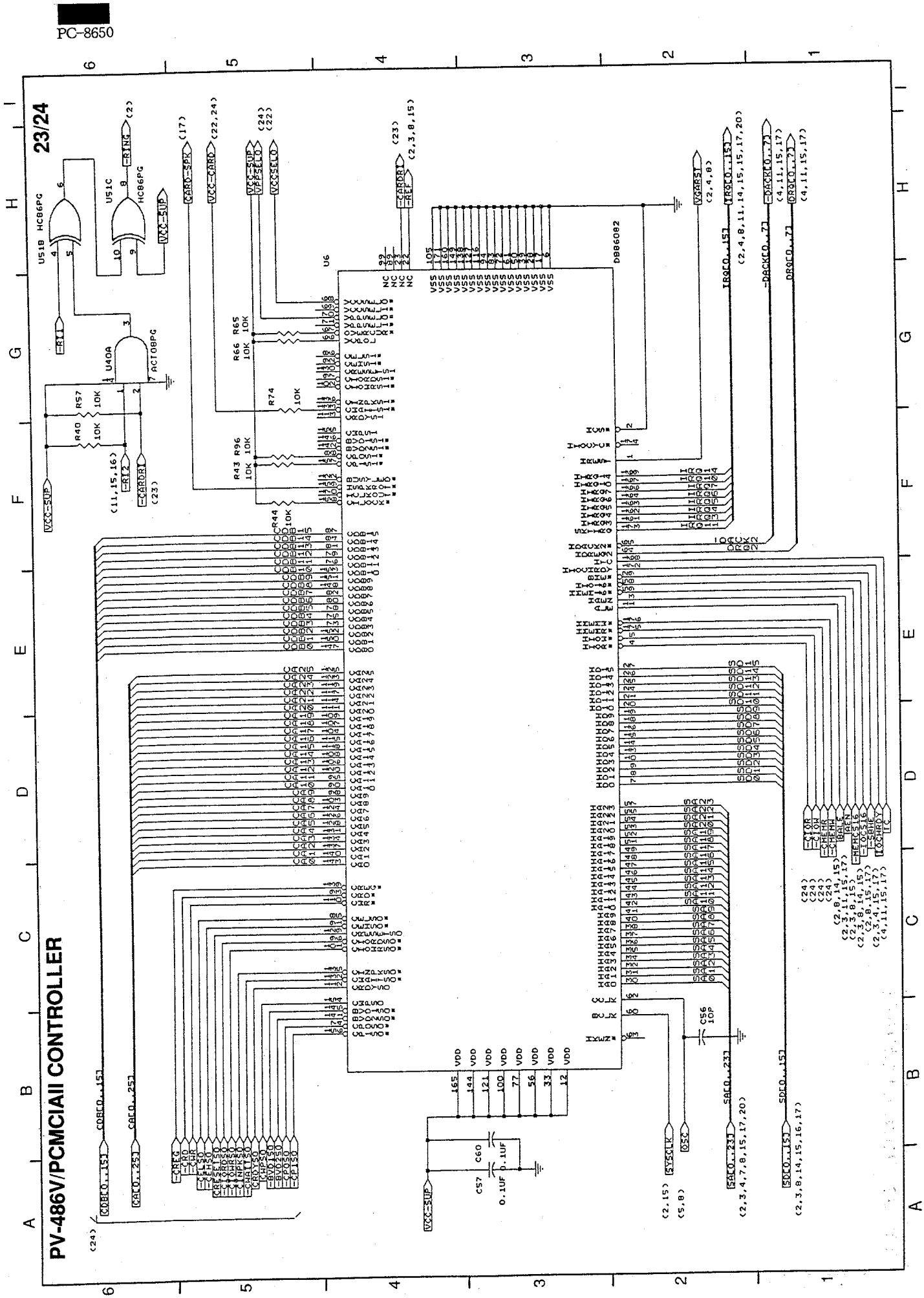
PV-486V/P52 MOUSE IRQ GENERATOR



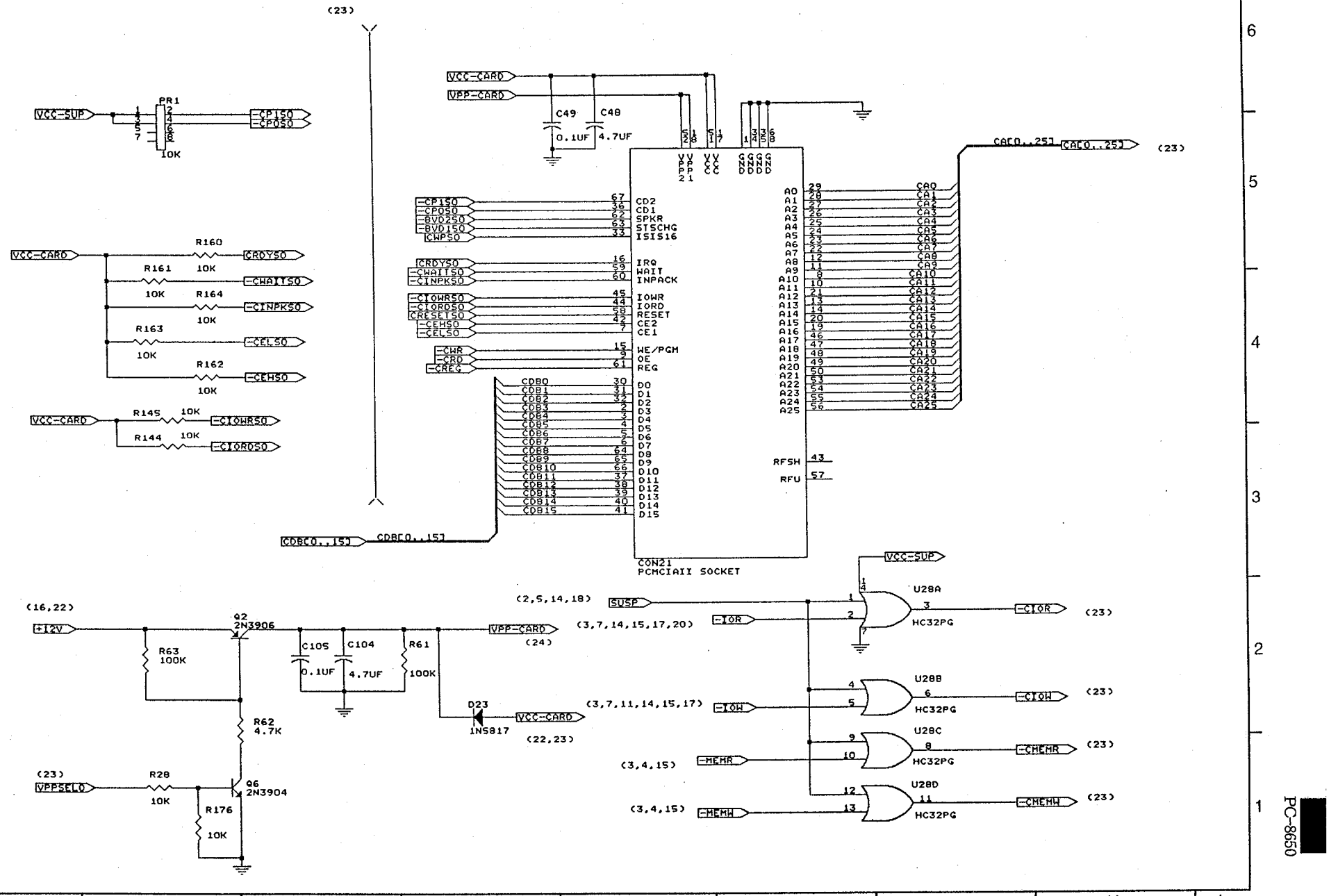

PV-486V/MEMORY CONNECTOR
21/24
MEMORY CON1
MEMORY CON2
CON13
CON9
C161
4.7UF
VCC-SUP
-BWEN
-BRAS
-BCAS1
-BCAS0
-BCAS3
-BCAS2
D0..31
BMA0..10
(1,2,6)
(3,6)
(3)

PV-486V/POWER CONTROL



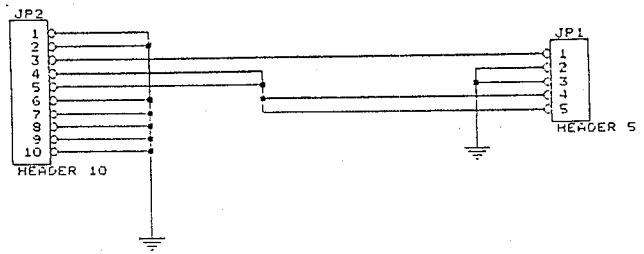

PV-486V/PCMCIAII CONTROLLER
23/24

PV-486V/PCMCIA II SOCKET



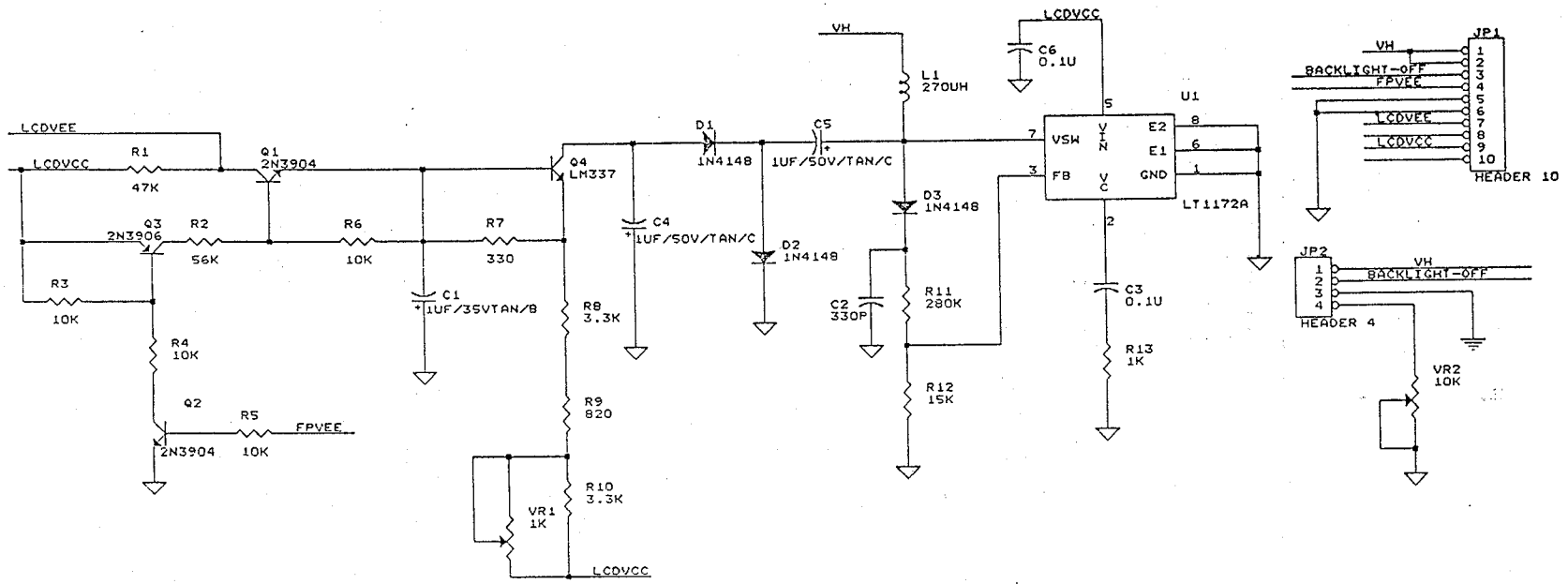
PV-TSP

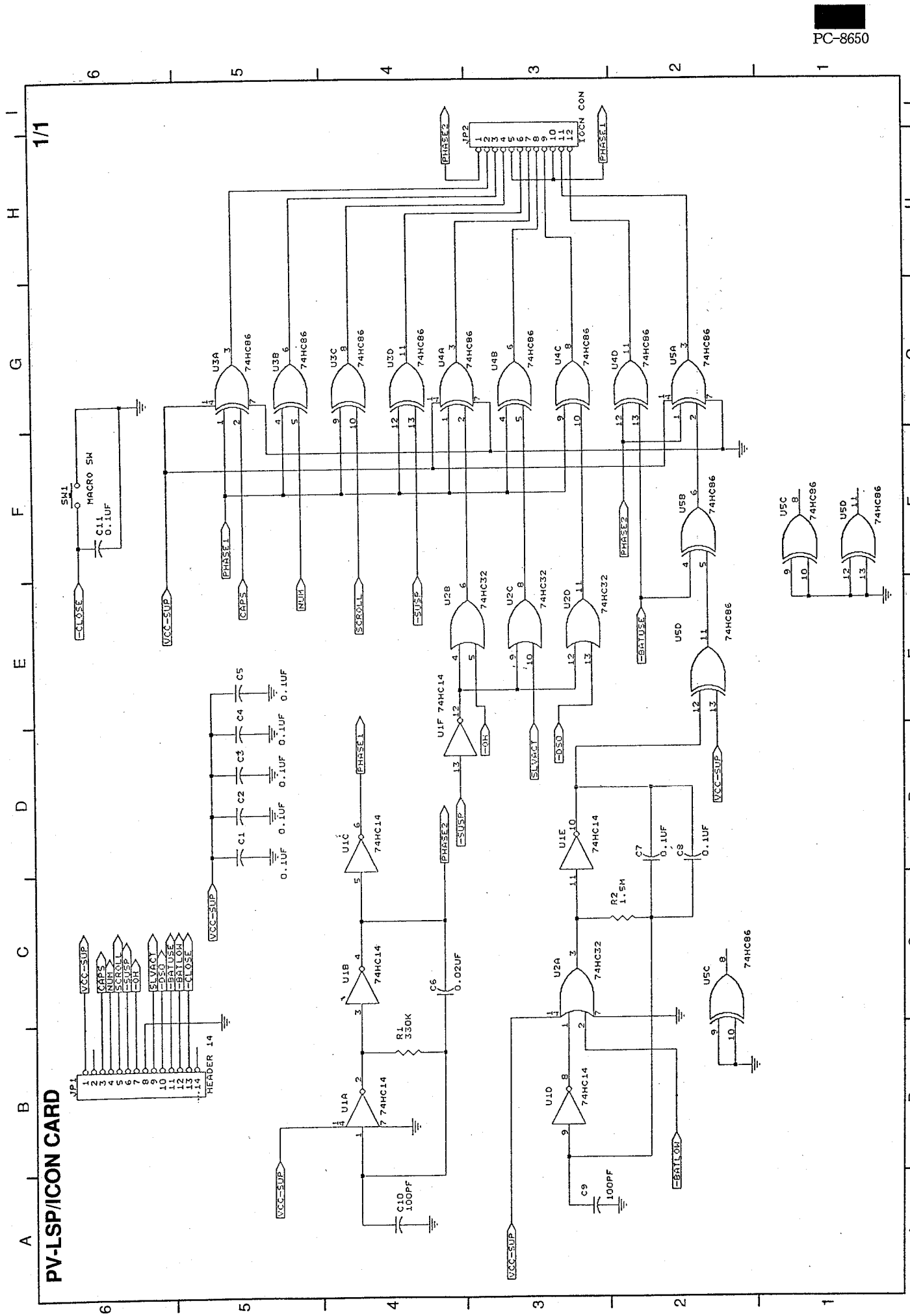
1/1

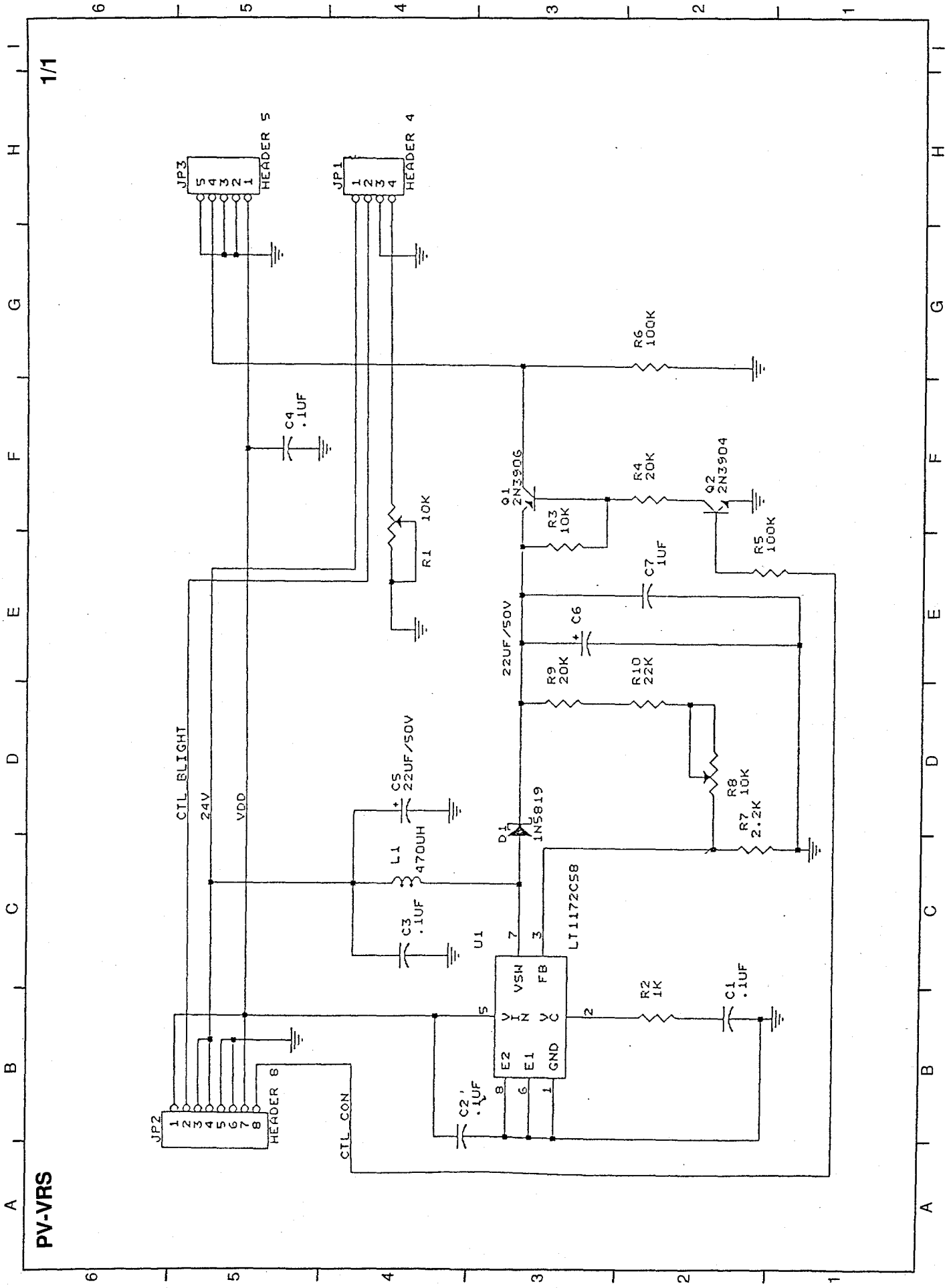


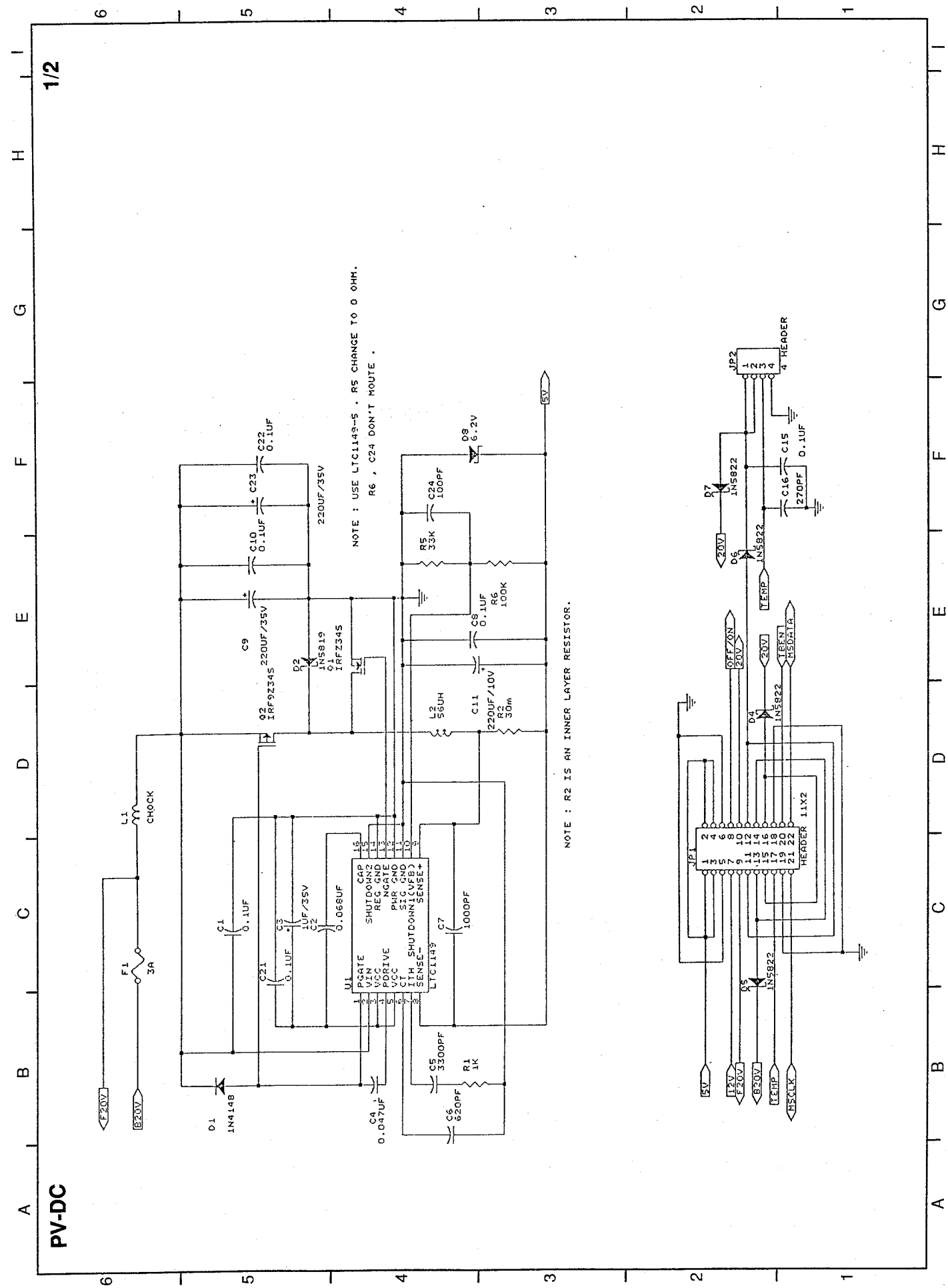
PV-VRM/CON/BRI

1/1



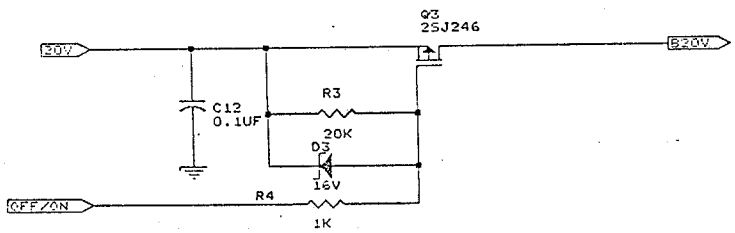

PV-LSP/ICON CARD
1/1
JP1
HEADER 14
VCC-SUP
CAPS
NUM
SCROLL
-SUSP
-OH
SLVACT
-DSO
-BATUSE
-BATLOW
-CLOSE
SW1
MACRO SW
C11 0.1UF
JP2
ICON CON
PHASE2
PHASE1
U3A 74HC86
U3B 74HC86
U3C 74HC86
U3D 74HC86
U4A 74HC86
U4B 74HC86
U4C 74HC86
U4D 74HC86
U5A 74HC86
U5B 74HC86
U5C 74HC86
U5D 74HC86
U5C 74HC86
U5D 74HC86
U5C 74HC86
U5D 74HC86
U2B 74HC32
U2C 74HC32
U2D 74HC32
U2A 74HC32
U1F 74HC14
U1C 74HC14
U1B 74HC14
U1A 74HC14
U1E 74HC14
U1D 74HC14
C1 0.1UF
C2 0.1UF
C3 0.1UF
C4 0.1UF
C5 0.1UF
C6 0.02UF
C7 0.1UF
C8 0.1UF
C9 100PF
C10 100PF
R1 330K
R2 1.5M

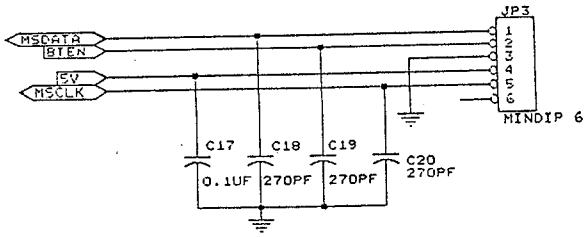

PV-VRS
1/1
JP3
HEADER 5
JP1
HEADER 4
JP2
HEADER 8
R6 100K
C4 .1UF
R1 10K
Q1 2N3906
R4 20K
Q2 2N3904
R3 10K
R5 100K
C7 1UF
C6 22UF/50V
R9 20K
R10 22K
R8 10K
R7 2.2K
C5 22UF/50V
L1 470UH
D1 1N5819
C3 .1UF
U1
LT1172CS8
VSW
FB
VIN
VC
E2
E1
GND
R2 1K
C1 .1UF
C2 .1UF
CTL_BLIGHT
24V
VDD
CTL_CON

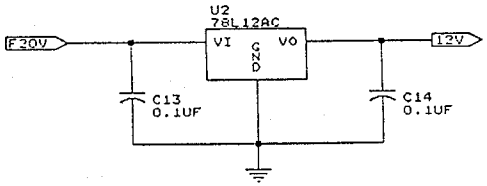

PV-DC
1/2
NOTE : USE LTC1149-5 , R5 CHANGE TO 0 OHM.
R6 , C24 DON'T MOUTE .
NOTE : R2 IS AN INNER LAYER RESISTOR.
F20V
B20V
5V
L1 CHOCK
F1 3A
D1 1N4148
C1 0.1UF
C21 0.1UF
C3 1UF/35V
C2 0.068UF
C4 0.047UF
C5 330PF
R1 1K
C6 620PF
C7 1000PF
U1 LTC1149
PGATE
VIN
VCC
PDRIVE
VCC
CT
ITH
SENSE-
CAP
SHUTDOWN2
REG GND
NGATE
PWR GND
SIG GND
SHUTDOWN1(VFB)
SENSE+
Q2 IRF9Z34S
D2 1N5819
Q1 IRFZ34S
C9 220UF/35V
C10 0.1UF
C23 220UF/35V
C22 0.1UF
L2 56UH
C11 220UF/10V
R2 30m
C8 0.1UF
R6 100K
R5 33K
C24 100PF
D8 6.2V
JP1 HEADER 11X2
JP2 4 HEADER
D7 1N5822
D6 1N5822
D4 1N5822
D5 1N5822
C15 0.1UF
C16 270PF
OFF/ON
TEEN
MSDATA
TEMP
MSCLK
12V
20V

PV-DC

2/2

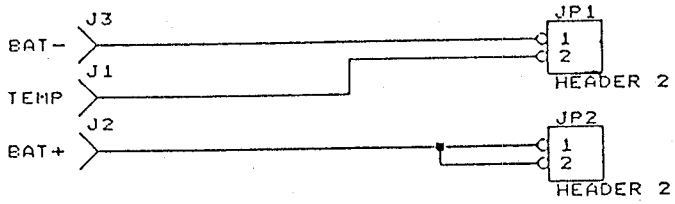






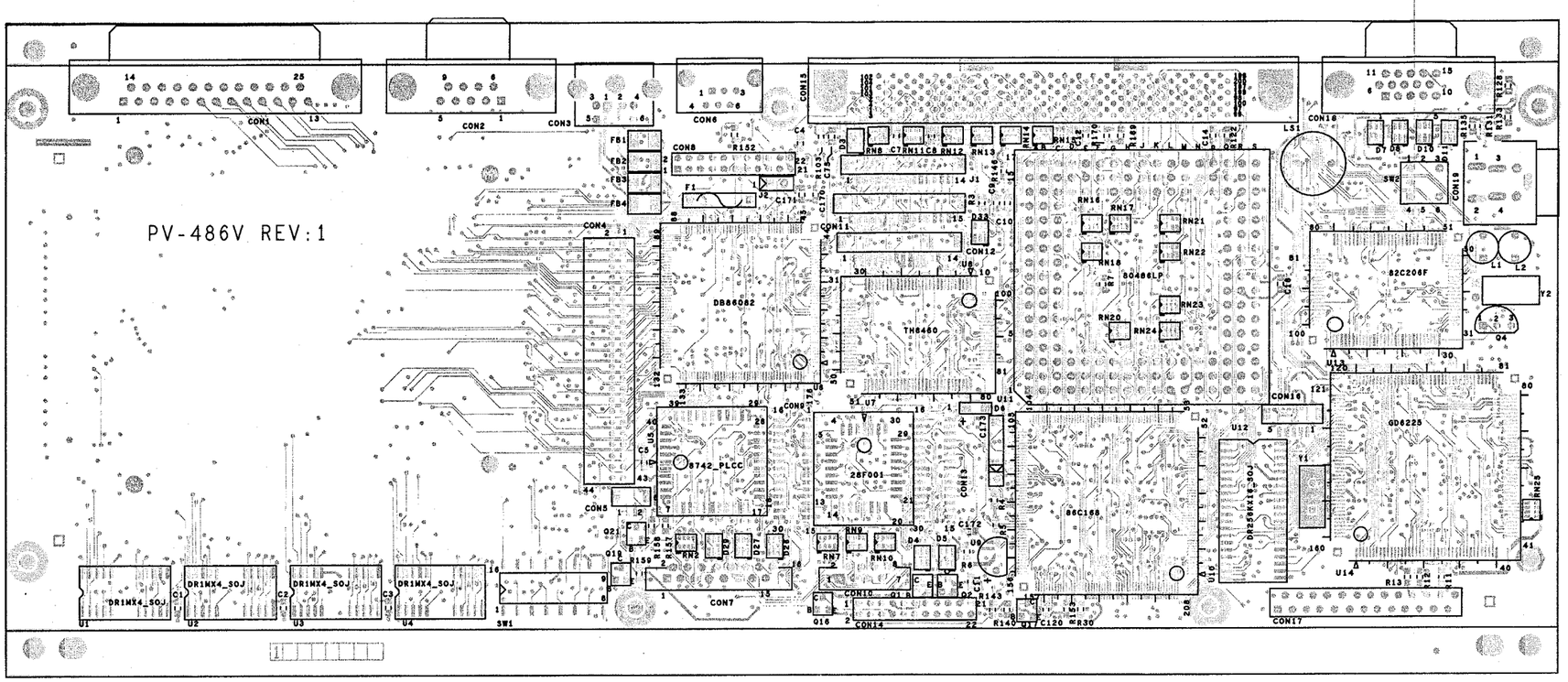
PE-BAT

1/1

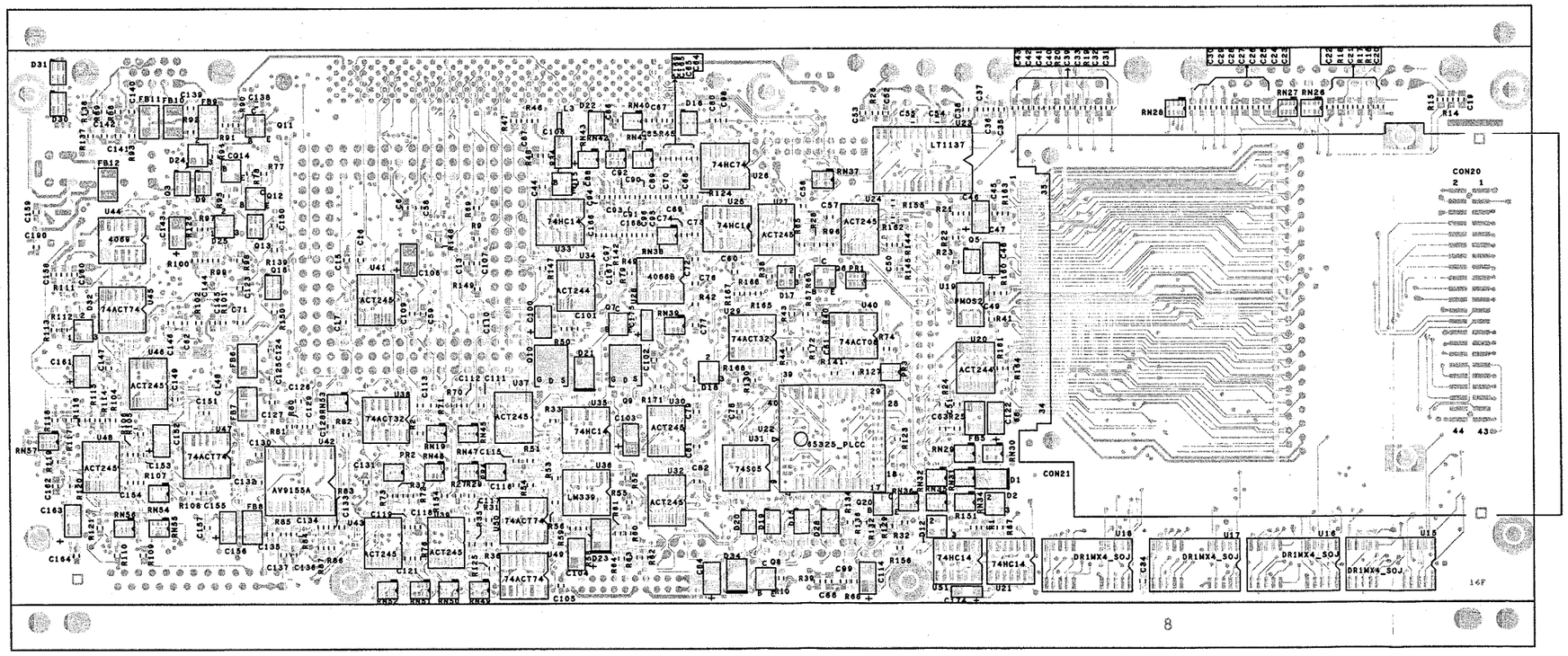


PARTS LAYOUT

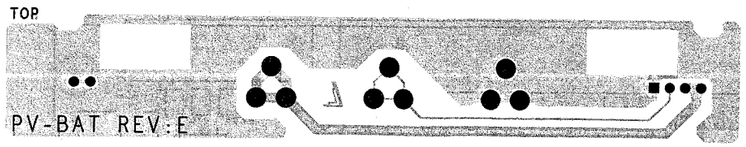
MAIN PWB - TOP VIEW



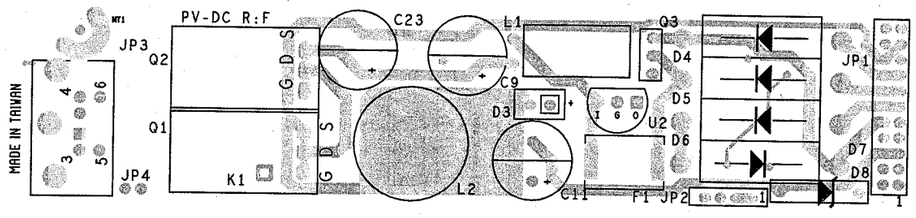
MAIN PWB - BOTTOM VIEW



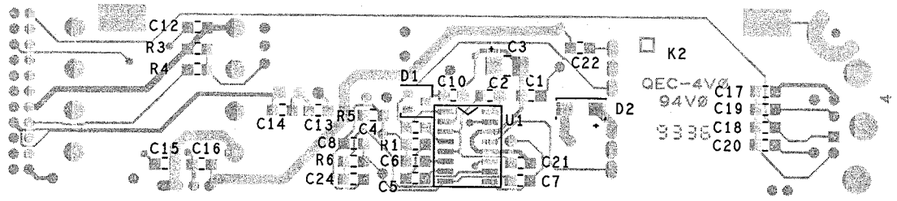
PV - BAT PWB



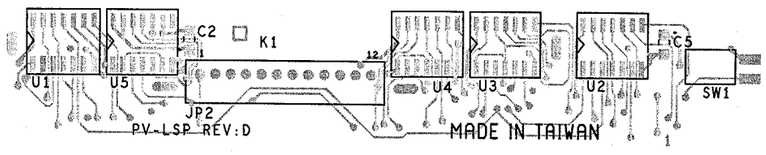
DC - DC PWB (TOP VIEW)



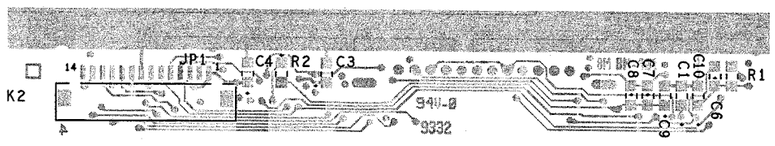
DC - DC PWB (BOTTOM VIEW)



LCD INDICATOR (TOP VIEW)

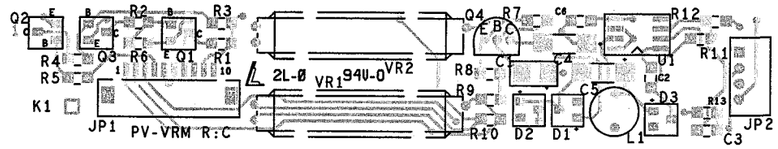


LCD INDICATOR (BOTTOM VIEW)



INTERFACE PWB (PC-8650)

VR PWB (PC-7850)



VR PWB (PC-8150)